32-bit CPU, 64kB Flash/10kB RAM, up to 25 fast I/O, 7 Timers,
4 Communication interfaces supporting LIN, 1 ADC, 1 DAC, 2 ACMPs, 3 OPAs, 2.0~5.5V

Features

- **32-bit CPU**
  - Up to 108MHz operating frequency
  - CORDIC co-processor
  - Hardware divider
  - Built-in electromotor acceleration algorithms
- **Memories**
  - 64kbytes embedded Flash (32-bit width), supporting prefetch and read/write protection, supporting parity check
  - 10kbytes SRAM (32-bit width) divided into two independent partitions of 4kbytes and 6kbytes, and supporting parity check
- **Reset and power management**
  - 2.0V to 5.5V power supply and I/O
  - Embedded two LDOs, one for core domains and another for low-power backup domains
  - High-precision power-on & power-down reset (POR_PDR)
  - Low-voltage reset circuit (LVR): 8 reset points are available (1.6V, 1.8V, 2.0V, 2.5V, 2.8V, 3.0V, 3.5V, 4.0V)
  - Low-voltage detection circuit (LVD): 8 detection points are available (2.0V, 2.2V, 2.4V, 2.7V, 2.9V, 3.1V, 3.6V, 4.5V)
- **Clock System**
  - Internal 16MHz factory-calibrated RC (RCH, 1% accuracy)
  - 32KHz low-speed oscillator crystal (OSCL)
  - Internal 32KHz factory-calibrated RC (RCL, 10% accuracy)
  - Internal PLL up to 256 MHz with jitter less than 100ps
- **Low power**
  - Sleep, Stop, ULP Stop mode
- **Debug mode**
  - Serial wire debug port (SW-DP)
- **Boot modes**
  - Boot from Flash or SRAM
- **Programming modes**
  - In-Circuit Serial Programming (ISP)
- **Up to 25 fast I/O ports**
  - All I/Os mapping to 16 external interrupt vectors and almost all 5V tolerant
  - Supporting input floating, input pull-up, input pull-down, output push-pull, output open-drain and output open-source
  - One or two analog channels for most IOs
  - I/O drive capability and slope are configurable in two levels
- **Seven timers**
  - One 16-bit advanced-control timer TIM1, 5 channels (with 4 complementary channels), supporting output comparison/PWM output/single-pulse output, dead-time control and emergency braking
  - One 16-bit general-purpose timer TIM2, 4 channels, supporting input capture/output comparison/PWM output/single -pulse output, quadrature (incremental) encoder input, hall detection and emergency braking
  - One 16-bit general-purpose timer TIM15, 2 channels (with 2 complementary channels), supporting input capture/output comparison/PWM output/single-pulse output, dead-time control and emergency braking

Address: Room 1501, Block A3, West Jianzhu Rd. 777, Binhu District, Wuxi, Jiangsu , China
Phone/Fax: 86-510-85388846

- One 16-bit general-purpose timer TIM16, 2 channels (with 1 complementary channels), supporting input capture/output comparison/PWM output/single-pulse output, dead-time control and emergency braking
- One 16-bit general-purpose timer TIM17, 1 channels (with 1 complementary channels), supporting input capture/output comparison/PWM output/single-pulse output, dead-time control and emergency braking
- One independent watchdog timer
- One 24-bit down-counter SysTick timer
- TIM1, TIM15, TIM16 and TIM17 support delay trigger and error-proof triggering mechanisms

- **Watch timer (WT)**
  - Supporting alarm clock and periodic wake-up
  - The buzz output with configurable frequencies
- **DMA**
  - 2 independent channels, 8 handshake signals
  - Supported peripherals: SPI, I2C, UART, ADC, DAC, Timers
- **CRC**
  - 8/16/32-bit configurable polynomials
- **DIV**
  - a 32/32 divider, 8 operation cycles, supporting signed calculation and downward compatibility 16/16
- **CORDIC**
  - Supporting trigonometric function, anti-trigonometric function, hyperbolic tangent function and rooting etc.
- **Up to 4 communication interfaces**
  - One I2C interface, supporting master/slave mode, 100K/400K/1Mbps rates, 7/10-bit addressing mode, supporting SMbus, supporting DMA with FIFO)
  - Two USART interfaces, supporting CTS/RTS hardware control, maximum baud rate of 4Mbps, supporting DMA with FIFO, low-power mode, and LIN 1.3/2.0/2.1/2.2/J2602 protocol by hardware
  - One SPI interface, supporting master/slave mode with frame size of 4 to 16 bit, and the Max. speed of master up to 32Mbps when slave up to 24Mbps, supporting DMA with FIFO
- **One 12-bit A/D converter**
  - Conversion rate up to 2 MSPS
  - 18 channels (16 external channels and 2 internal channels)
  - Built-in temperature sensor VTS
  - Supporting internal and external reference voltages: 3.2V (when VDDA>2.2V), 4.9V (when VDDA>4V) or VDDA
  - Two sampling/hold circuits with flexible SOC mode, supporting ADC channel pending and injection
- **One 10-bit D/A converter**
  - Configurable reference voltage
  - Supporting hardware triggering and DMA transmission, supporting noise or triangular waveform generation
- **Two analog comparators (ACMP)**
  - Internal or external input
  - Built-in HALL-MID restoration module with observable output
- **Three operational amplifiers (OPA)**
  - OPA 0/1/2 Magnification: 1/2/4/6/8/10/16/32
  - Supporting 2 external inputs or internal ground
- **Operating temperature**
  - Ambient temperature: -40°C ~ +125°C
- **128-bit unique ID**

1. Function Overview

1.1 YTM32U067A

YTM32U067A series is mainly used for applications such as motor control, integrating three independent PMOS, three independent NMOS gate drive modules, and a 5.0V50mA LDO integrated module.

The pre-driver module of YTM32U067A is YTD31A02.

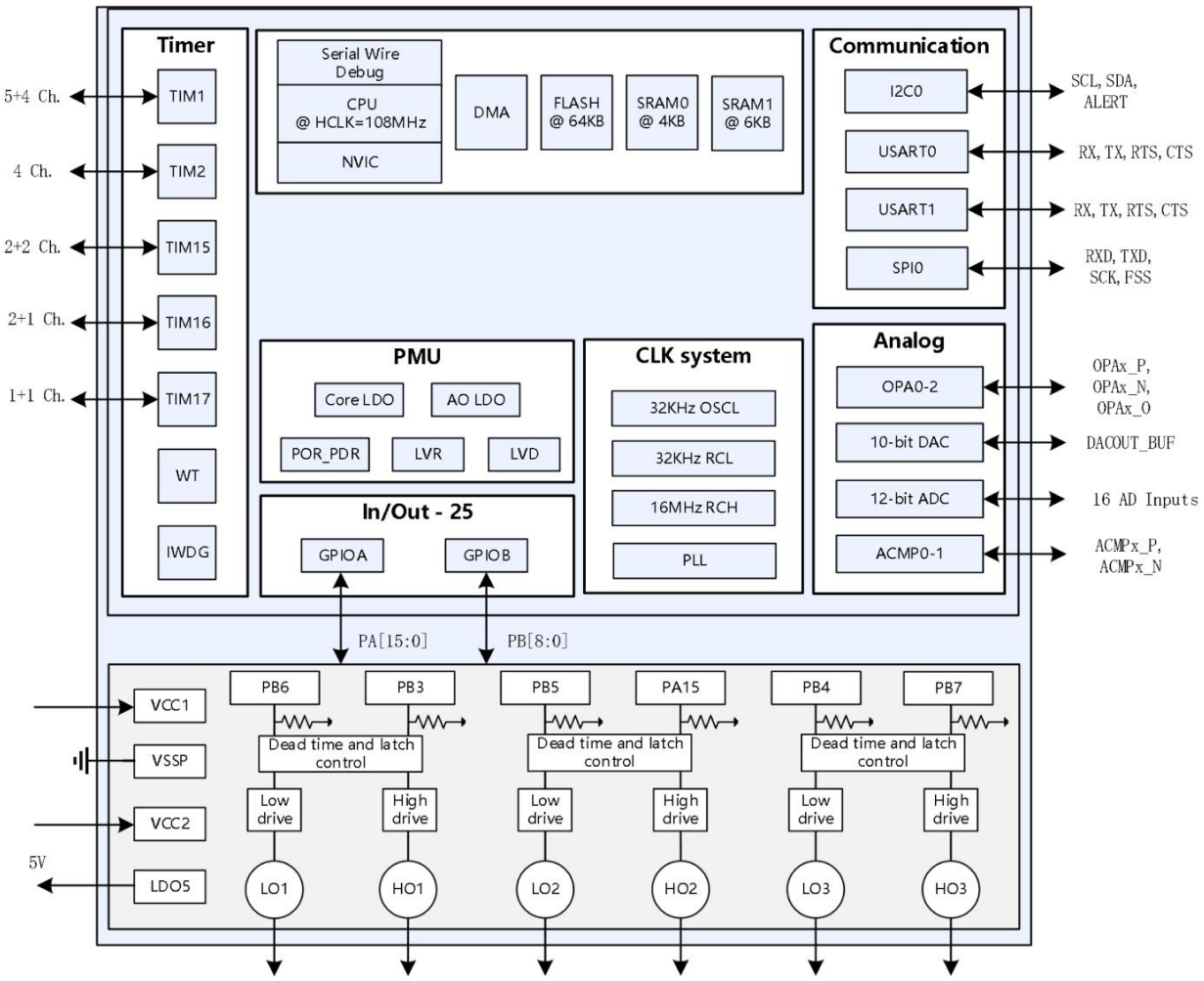


Figure 1- 1 Block diagram of YTM32U067A

1.2 Pre-Driver YTD31A02

YTD31A02 is a three-phase high-speed power MOSFET driver with 6 channels and up to 40V operating voltage. Using high and low voltage compatibility process enables the high and low gate drive circuits to be integrated in a single chip. CMOS or LSTTL outputs are logic compatible and logic inputs can be down to 3.3V.

In addition, a built-in dead-time control function is used to avoid cross-conduction on the high side. The pre-driver module outputs a 10V gate supply voltage for PMOS and NMOS. In order to simplify the PCB design, a 5V/50mA LDO is integrated to power MCU. The pre-driver module also integrates thermal shutdown protection for safety reasons.

Features:

- P/N MOS half-bridge three-phase output
- Power supply voltage 5V~28V which can up to 40V
- Adapt to 3.3V-20V input voltage
- Built-in 5V/50mA LDO
- Output current capability: IO +/- 0.05A/0.3A
- Built-in VCC under-voltage lockout
- Built-in 130ns dead-time control
- Integrated latch-off function
- Ambient temperature: -40°C ~ +125°C
- Built-in over-temperature protection
- The input channels of LIN1/2/3 are active high and control LO output
- The input channels of HIN1/2/3 are active high and control HO output

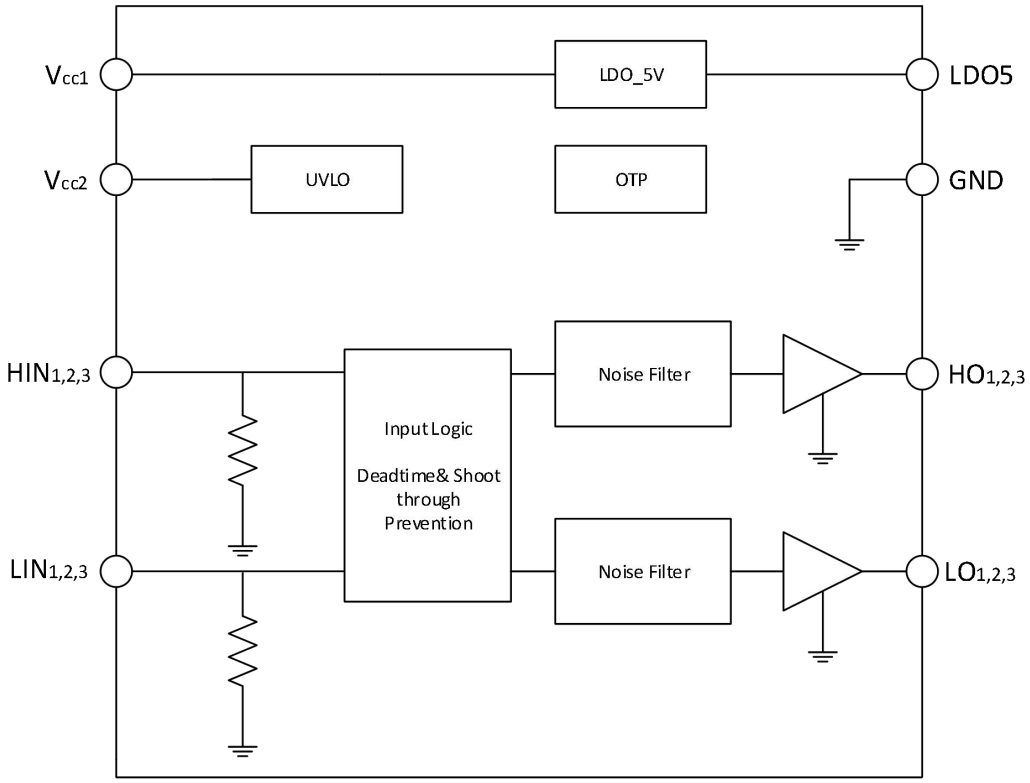


Figure 1- 2 Block diagram of YTD31A02

2. Pinouts and Pin Descriptions

Table 2- 1 Abbreviations used for pin definitions

Name		Abbr.	Description
Pin Name		The pin function and name stay the same during/after reset unless specifically stated in brackets	
Pin Type		S	Power pin
		I	Only input pin
		I/O	Input/output pin
I/O Structure		2ANA	Two analog alternate channels and two normal analog switches (PAD to analog switches with ESD resistance)
		2ANA_OP	Two analog alternate channels, one normal analog switch and one analog switch of low inner resistance
		2OP	Two analog alternate channels and two analog switches of low inner resistance (PAD directly to analog switch for OPA)
Note		All I/Os are floating input during/after reset, unless specified in *Note*	
Pin Function	Optional alternate function	Features configured by GPIOx_AFL/H, GPIOx_MODE registers (digital alternate)	
	External alternate function	Features configured by the SYSCTRL register which has higher priority than optional alternate function (digital alternate)	
	Analog alternate function1	Analog function 1 configured by SYSCTRL or GPIOx_AFL/H, GPIOx_MODE registers	
	Analog alternate function 2	Analog function 2 configured by SYSCTRL or GPIOx_AFL/H, GPIOx_MODE registers	

2.1 YTM32U067A Pin Definition

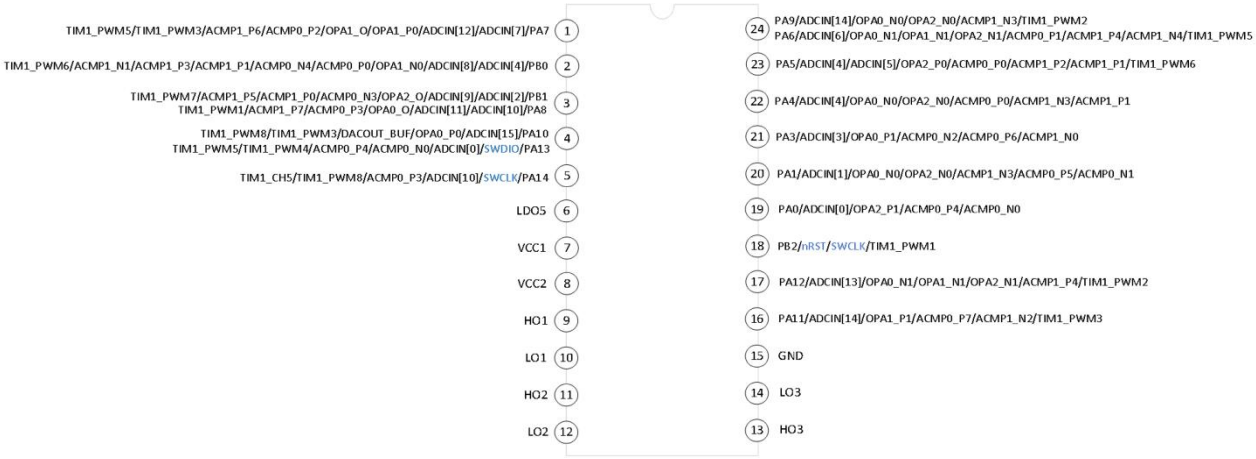


Figure 2- 1 Pinout

(The details of pins refer to Table 2-2)

Table 2- 2 Pin definitions

Pin name	Pin type	I/O structure	Optional alternate function	External alternate function	Analog alternate function (AN)	
					YA1	YA2
PB7	I/O	2ANA	TIM1_PWM2 TIM1_PWM3 TIM1_PWM6 TIM17_CH1 TIM17_CH1N I2C0_SDA USART0_RX USART0_TX		ADCIN[8] OPA1_N0 ACMP0_N4 ACMP1_P3 ACMP1_N1 (PB0_YA2)	
PB8 (BOOT0)	I/O	2ANA	TIM1_PWM2 TIM1_PWM3 TIM1_PWM5 TIM15_CH2 TIM16_CH1 TIM17_CH1N TIM17_ETR I2C0_ALERT	BOOT[1]	ADCIN[13] (PA2_YA1/ PA12_YA2/ PB5_YA2)	ADCIN[14] (PA9_YA2/ PA11_YA2)
PA11	I/O	2OP	TIM1_PWM3 TIM15_CH1 I2C0_SDA USART0_TX USART0_CTS WT_Buz		OPA1_P1 ACMP0_P7 ACMP1_N2	ADCIN[14] OSCL_OUT (PA9_YA2/ PB8_YA2)
PA12	I/O	2OP	TIM1_PWM2 TIM15_CH1N I2C0_SCL		OPA0_N1 OPA1_N1 OPA2_N1	ADCIN[13] OSCL_IN (PA2_YA1/

			USART0_RX USART0_RTS WT_nBuz		ACMP1_P4 (PA6_YA2)	PB5_YA2/ PB8_YA1)
PB2 (nRST)	I/O	2ANA	TIM1_PWM1 TIM2_CH3 TIM15_CH2 TIM16_CH1N TIM1/2/15/16/17_GPI O_BKIN USART0_TX USART1_TX	SWCLK[2] nRST[3]		
VSS	S					
VSSA	S					
PA2	I/O	2ANA_OP	TIM1_PWM4 TIM1_PWM5 TIM15_CH2 USART1_RX USART1_TX SPI0_RXD SPI0_TXD ACMP0_out		ADCIN[13] (PA12_YA2/ PB5_YA2/ PB8_YA1)	ADCIN[2] OPA2_O ACMP1_P5 (PB1_YA2)
VDDH	S					
VDDA	S					
PA0	I/O	2ANA_OP	TIM2_CH1 TIM16_CH1 TIM1_ETR TIM15_ETR I2C0_ALERT USART1_RX USART1_CTS ACMP0_out		ADCIN[0] ACMP0_P4 ACMP0_N0 (PA13_YA1)	OPA2_P1
PA1	I/O	2ANA_OP	TIM2_CH2 TIM15_CH1N TIM16_CH1N TIM16_CH2 TIM16_ETR I2C0_SDA USART1_RTS USART1_TX		ADCIN[1] ACMP0_P5 ACMP0_N1 OPA1_OX (PA15_YA1)	OPA0_N0 OPA2_N0 ACMP1_N3 (PA4_YA2/ PA9_YA1)
PA3	I/O	2ANA_OP	TIM2_CH3 TIM15_CH1 I2C0_SCL USART1_TX USART1_RX		ADCIN[3] ACMP0_N2 ACMP0_P6 ACMP1_N0	OPA0_P1

			SPI0_RXD SPI0_TXD ACMP1_out			
PA5	I/O	2ANA_OP	TIM1_PWM6 TIM15_CH1 TIM16_CH2 TIM2_ETR TIM15_ETR I2C0_SCL SPI0_SCK WT_nBuz		ADCIN[4] ACMP0_P0 ACMP1_P1 (PA4_YA1/ PB0_YA1/ PB4_YA1)	ADCIN[5] OPA2_P0 ACMP1_P2 (PB3_YA1)
PA4	I/O	2ANA_OP	TIM15_CH2 TIM17_CH1 USART0_RTS USART1_TX USART1_CK SPI0_FSS ACMP1_out WT_Buz		ADCIN[4] ACMP0_P0 ACMP1_P1 (PA5_YA1/ PB0_YA1/ PB4_YA1)	OPA0_N0 OPA2_N0 ACMP1_N3 (PA1_YA2/ PA9_YA1)
PA7	I/O	2OP	TIM1_PWM3 TIM1_PWM5 TIM2_CH2 TIM17_CH1 USART0_RX SPI0_RXD SPI0_TXD ACMP1_out		ADCIN[7] OPA1_P0 ACMP0_P2 (PB6_YA1)	ADCIN[12] OPA1_O ACMP1_P6
PA6	I/O	2ANA_OP	TIM1_PWM5 TIM2_CH1 TIM16_CH1 TIM1_GPIO_BKIN USART0_CK SPI0_RXD SPI0_TXD ACMP0_out		ADCIN[6] ACMP0_P1 ACMP1_N4 (PB5_YA1)	OPA0_N1 OPA1_N1 OPA2_N1 ACMP1_P4 (PA12_YA1)
PB0	I/O	2ANA_OP	TIM1_PWM6 TIM2_CH3 USART0_RX USART0_TX EVENTOUT		ADCIN[4] ACMP0_P0 ACMP1_P1 (PA4_YA1/ PA5_YA1/ PB4_YA1)	ADCIN[8] OPA1_N0 ACMP1_P3 ACMP1_N1 ACMP0_N4 (PB7_YA1)
PB1	I/O	2ANA_OP	TIM1_PWM7 TIM2_CH4 TIM15_CH1		ADCIN[9] ACMP0_N3 ACMP1_P0	ADCIN[2] OPA2_O ACMP1_P5

			I2C0_ALERT USART0_RX USART0_TX USART1_RTS		OPA2_OX (PB6_YA2)	(PA2_YA2)
PA8	I/O	2ANA_OP	TIM1_PWM1 TIM15_CH2 TIM16_GPIO_BKIN TIM17_ETR USART0_TX USART0_CTS ACMP0_out MCO		ADCIN[10] ACMP0_P3 OPA0_OX ELVI[4] (PA14_YA1)	ADCIN[11] OPA0_O ACMP1_P7
PA9	I/O	2ANA_OP	TIM1_PWM2 TIM15_CH1 TIM15_CH2N TIM15_GPIO_BKIN TIM16_GPIO_BKIN I2C0_SCL USART0_RX USART0_TX		OPA0_N0 OPA2_N0 ACMP1_N3 (PA1_YA2/ PA4_YA2)	ADCIN[14] (PA11_YA2/ PB8_YA2)
PA10	I/O	2ANA_OP	TIM1_PWM3 TIM1_PWM8 TIM15_CH2 TIM1_GPIO_BKIN TIM17_GPIO_BKIN I2C0_SDA USART0_RX USART0_TX		ADCIN[15] OPA0_P0	DACOUT_BUF (PA13_YA2)
PA13	I/O	2ANA	TIM1_PWM4 TIM1_PWM5 TIM16_CH1 I2C0_SDA USART1_RX ACMP1_out IR_OUT	SWDIO[2]	ADCIN[0] ACMP0_P4 ACMP0_N0 (PA0_YA1)	DACOUT_BUF (PA10_YA2)
PA14	I/O	2ANA	TIM1_PWM8 TIM1_CH5 TIM17_CH1 TIM1_GPIO_BKIN I2C0_SCL USART1_RX USART1_TX	SWCLK[2]	ADCIN[10] ACMP0_P3 OPA0_OX ELVI[4] (PA8_YA1)	PMU_AOUT (PA15_YA2)
PA15	I/O	2ANA	TIM1_PWM1 TIM1_PWM4		ADCIN[1] ACMP0_P5	PMU_AOUT[6] (PA14_YA2)

			TIM16_CH1N TIM17_CH1 TIM1_GPIO_BKIN TIM15_GPIO_BKIN USART1_RX SPI0_FSS		ACMP0_N1 OPA1_OX (PA1_YA1)	
PB3	I/O	2ANA	TIM1_PWM1 TIM1_PWM5 TIM1_PWM8 TIM1_PWM7 TIM16_CH1 TIM16_ETR USART1_TX SPI0_SCK		ADCIN[5] OPA2_P0 ACMP1_P2 (PA5_YA2)	
PB4	I/O	2ANA	TIM1_PWM6 TIM1_PWM7 TIM2_CH1 TIM16_CH2 TIM17_GPIO_BKIN USART0_RX SPI0_RXD SPI0_TXD		ADCIN[4] ACMP0_P0 ACMP1_P1 (PA4_YA1/ PA5_YA1/ PB0_YA1)	
PB5	I/O	2ANA_OP	TIM1_PWM3 TIM1_PWM4 TIM1_PWM6 TIM1_PWM8 TIM2_CH2 USART0_TX SPI0_RXD SPI0_TXD		ADCIN[6] ACMP0_P1 ACMP1_N4 (PA6_YA1)	ADCIN[13] (PA2_YA1/ PA12_YA2/ PB8_YA1)
PB6	I/O	2ANA	TIM1_PWM1 TIM1_PWM5 TIM2_CH3 TIM15_CH2 TIM16_CH1N I2C0_SCL USART0_RX USART0_TX		ADCIN[7] OPA1_P0 ACMP0_P2 (PA7_YA1)	ADCIN[9] ACMP0_N3 ACMP1_P0 OPA2_OX (PB1_YA1)
VDDH	S					
VDDA	S					
LDO5	P				5V power output of pre-driver module	
VCC1	P				5V power input of pre-driver module	
VCC2	O				Drive power input of pre-driver module	
HO1	O				High-side output 1 of pre-driver module	

LO1	O				Low-side output 1 of pre-driver module
HO2	O				High-side output 2 of pre-driver module
LO2	O				Low-side output 2 of pre-driver module
HO3	O				High-side output 3 of pre-driver module
LO3	O				Low-side output 3 of pre-driver module
GND	P				Ground of pre-driver module

Note1: *According to the option byte configuration, it can be used as a BOOT0 pin during system reset to select the boot mode, then can be used for normal function.*

Note2: *According to the option byte configuration, one of SWCLK (PB2 or PA14) pins and SWDIO (PA13) can be selected during system reset. After that SWDIO pin is pulled up internally and the SWCLK pin is pulled down internally.*

Note3: *After power-on reset, the PB2 pin is configured as an external reset pin nRST by default. If the option byte is configured as SWCLK, PB2 will be used as SWCLK when the chip starts working, meantime the external reset configuration will be automatically turned off, and then configured by software.*

Note4: *ELVI is an external voltage that can be detected by LVD.*

Note5: *The I/O drive strength 4mA/8mA when powered by 3.3V, and 8mA/16mA when powered by 5V.*

Note6: *PMU_AOUT is the power supply observation output of the chip.*

Table 2- 3 Pre-driver pin connection

Drive output pin	Drive input pin	Pin description	Internal connection	Example of corresponding TIM1 PWM functions	
HO1	HIN1	The logic input control signal is active at high, and control MOS high-side: "0" is to turn off the power MOS, "1" is turn on the power MOS.	PB3	AF6	TIM1_PWM1
HO2	HIN2		PA15	AF7	TIM1_PWM4
HO3	HIN3		PB7	AF5	TIM1_PWM3
LO1	LIN1	The logic input control signal is active at high, and control MOS low-side: "0" is to turn off the power MOS, "1" is to turn on the power MOS.	PB6	AF4	TIM1_PWM5
LO2	LIN2		PB5	AF6	TIM1_PWM6
LO3	LIN3		PB4	AF4	TIM1_PWM7

3. Memory Mapping

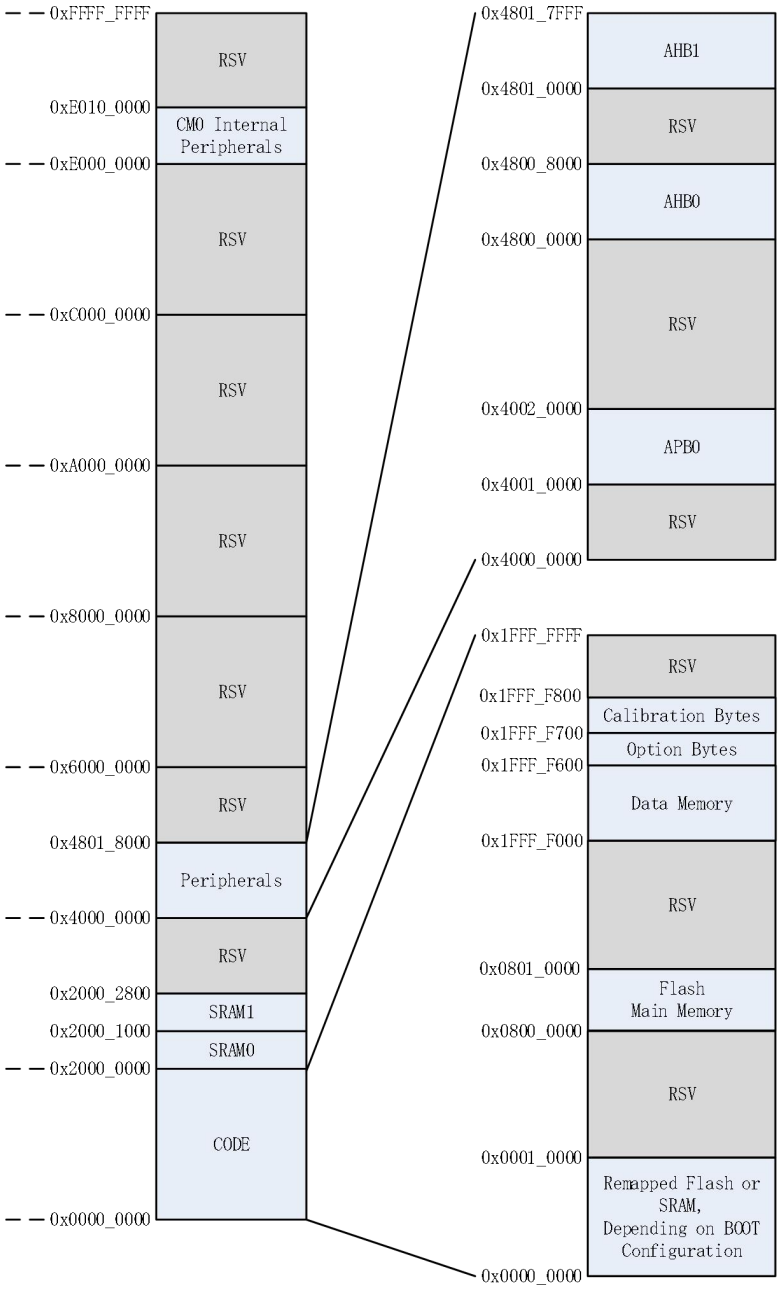


Figure 3- 1 Memory mapping

Table 3- 1 Register boundary addresses

Bus	Address Area	Size	Peripheral
APB0	0x4001_0000 - 0x4001_0FFF	4KB	TIM1
	0x4001_1000 - 0x4001_1FFF	4KB	EXTI
	0x4001_2000 - 0x4001_2FFF	4KB	Reversed
	0x4001_3000 - 0x4001_3FFF	4KB	I2C0
	0x4001_4000 - 0x4001_4FFF	4KB	USART0
	0x4001_5000 - 0x4001_5FFF	4KB	USART1
	0x4001_6000 - 0x4001_6FFF	4KB	Reversed

	0x4001_7000 - 0x4001_73FF	1KB	CHIPCTRL
	0x4001_7400 - 0x4001_77FF	1KB	IWDG
	0x4001_7800 - 0x4001_7BFF	1KB	WT
	0x4001_7C00 - 0x4001_7FFF	1KB	ANA CTRL
	0x4001_8000 - 0x4001_8FFF	4KB	SPI0
	0x4001_9000 - 0x4001_9FFF	4KB	Reversed
	0x4001_A000 - 0x4001_AFFF	4KB	ADC
	0x4001_B000 - 0x4001_BFFF	4KB	TIM15
	0x4001_C000 - 0x4001_CFFF	4KB	TIM16
	0x4001_D000 - 0x4001_DFFF	4KB	FLASH CTRL
	0x4001_E000 - 0x4001_EFFF	4KB	TIM17
	0x4001_F000 - 0x4001_FFFF	4KB	TIM2
	0x4002_0000 - 0x47FF_FFFF	~128MB	Reversed
AHB0	0x4800_0000 - 0x4800_01FF	512B	GPIOA
	0x4800_0200 - 0x4800_03FF	512B	GPIOB
	0x4800_0400 - 0x4800_05FF	512B	Reversed
	0x4800_0600 - 0x4800_07FF	512B	Reversed
	0x4800_0800 - 0x4800_09FF	512B	Reversed
	0x4800_0A00 - 0x4800_0BFF	512B	Reversed
	0x4800_0C00 - 0x4800_0DFF	512B	Reversed
	0x4800_0E00 - 0x4800_0FFF	512B	Reversed
	0x4800_1000 - 0x4800_1FFF	4KB	Reversed
	0x4800_2000 - 0x4800_2FFF	4KB	Reversed
	0x4800_3000 - 0x4800_3FFF	4KB	Reversed
	0x4800_4000 - 0x4800_4FFF	4KB	DMA
	0x4800_5000 - 0x4800_5FFF	4KB	Reversed
	0x4800_6000 - 0x4800_6FFF	4KB	Reversed
	0x4800_7000 - 0x4800_7FFF	4KB	SYS CTRL
	0x4800_8000 - 0x4800_FFFF	32KB	Reversed
AHB1	0x4801_0000 - 0x4801_0FFF	4KB	CORDIC
	0x4801_1000 - 0x4801_1FFF	4KB	CRC
	0x4801_2000 - 0x4801_2FFF	4KB	Reversed
	0x4801_3000 - 0x4801_3FFF	4KB	Reversed
	0x4801_4000 - 0x4801_4FFF	4KB	Reversed
	0x4801_5000 - 0x4801_5FFF	4KB	DIV
	0x4801_6000 - 0x4801_6FFF	4KB	Reversed
	0x4801_7000 - 0x4801_7FFF	4KB	Reversed

4. Electrical Characteristics

4.1 Absolute Characteristics

Table 4- 1 YTD31A02 absolute characteristics

Parameter	Symbol	Min.	Max.	Unit
Supply voltage	VCC1, VCC2	-0.3	40	V
5V output voltage	V_{5V}	-0.3	6	V
5V output current	I_{5V}	-0.3	50	mA
High-side output	HO1, HO2, HO3	VCC2-15	VCC2	V
Low-side output	LO1, LO2, LO3	-0.3	15	V
High-side input level	HIN1, HIN2, HIN3	-0.3	20	V
Low-side input level	LIN1, LIN2, LIN3	-0.3	20	V
Ambient temperature	T_A	-40	125	°C
Storage temperature	T_{STG}	-55	150	°C

Note: *Stresses above the absolute maximum values may cause permanent damage to the device. Exposure to maximum value conditions for extended periods may affect device reliability.*

4.2 Typical Characteristics

Unless otherwise specified, T_A=25°C, VCC1=VCC2=24V, load capacitance C_L=1nF.

Table 4- 2 YTD31A02 typical characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	VCC1, VCC2	-	5	-	28	V
5V output voltage	V_{5V}	-	4.7	5	5.3	V
5V output current	I_{5V}	VCC1=10V~28V	0	-	50	mA
Input frequency	f_{IN}	-	0	-	50	kHz
HIN and LIN logic input ON threshold voltage	$V_{IN,ON}$	-	2.9	-	VCC2	V
HIN and LIN logic input OFF threshold voltage	$V_{IN,OFF}$	-	0	-	0.4	V
Dead time between HIN and LIN	t_{DT}	-	0.5	-	-	us
Static characteristics						
High level input threshold voltage	V_{IH}	-	2.5	-	-	V
Low level input threshold voltage	V_{IL}	-	-	-	0.8	V
Input logic 1 bias current	I_{IN+}	-	-	36	100	uA
Input logic 0 bias current	I_{IN-}	-	-	0	1	uA
HO high level output voltage	$V_{HO,OH}$	-	-	VCC2	-	V
HO low level output voltage	V_{HO_OL}	-	VCC2-11.5	VCC2-10	VCC2-8.5	V
LO high level output voltage	$V_{LO,OH}$	-	8.5	10	11.5	V
LO low level output voltage	V_{LO_OL}	-	-	0	-	V
Output high short-circuit pulse current	I_{O+}	-	-	50	-	mA
Output low short-circuit pulse	I_{O-}	-	-	300	-	mA

current						
VCC under-voltage positive threshold	V_{CCUV+}	-	3.8	4.5	5	V
VCC under-voltage negative threshold	V_{CCUV-}	-	3.6	4.3	4.8	V
Hysteresis of VCC under-voltage	V_{CCHYS}	-	0.1	0.2	0.4	V
VCC static current	I_{QCC}	-	0.3	0.5	1.0	mA
Thermal shutdown temperature	T_{SD+}	-	-	150	-	°C
Restore temperature after thermal shutdown	T_{SD-}	-	-	135	-	°C
Dynamic characteristics						
On delay	T_{on}	-	-	80	-	ns
Off delay	T_{off}	-	-	30	-	ns
Dead time	DT	-	-	130	-	ns
Rise time	T_r	-	-	300	-	ns
Fall time	T_f	-	-	60	-	ns
Matching delay time	MT	-	-	80	-	ns

4.3 YTM32U067AS24

4.3.1 Absolute Maximum Values

Stresses above the absolute maximum values may cause permanent damage to the device. These values are operating conditions, and it is recommended to use the device in the scope of these specifications. Exposure to maximum value conditions for extended periods may affect device reliability.

Table 4- 3 Voltage characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDDH/VDDA	-0.3	3.3/5	6.5	V
I/O input voltage	V_{IN}	-0.3	3.3/5	5.8	V

Note: *All the voltages listed are referenced with VSS.*

Table 4- 4 Current characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Total current into VDDH/VDDA	$\sum I_{VDD}$	-	-	-	120	mA
Total current out of VSS/VSSA	$\sum I_{VSS}$	-	-	-	-120	
Max. current of each VDDH/VDDA	I_{VDD} (pin)	-	-	-	100	
Max. current of each VSS/VSSA	I_{VSS} (pin)	-	-	-	-100	
Injected current on IO	I_{INJ}	$V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$	-10	10	20	
Total injected current	ΣI_{INJ}	-	-50	-	50	

Table 4- 5 Thermal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Ambient temperature	T_{STG}	-65	25	125	℃
Junction temperature	T_J	-	25	150	

4.3.2 Operating Conditions

4.3.2.1 Recommended operating conditions

Table 4- 6 Operating conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	VDDH	-	2.0	3.3/5	5.5	V
Analog supply voltage	VDDA	>= VDDH	2.0	3.3/5	5.5	V
I/O input voltage	V_{IN}	-	-0.3	-	5.5	V
CPU frequency	f_{CPU}	VDDH＞2.0V	-	-	108	MHz
AHB clock frequency	f_{AHB}	-	-	-	108	MHz
APB clock frequency	f_{APB}	-	-	-	48	MHz
VDDH/VDDA rising rate	t_{VRISE}	-	0	-	∞	us/V
VDDH/VDDA falling rate	t_{VFALL}	-	20	-	∞	us/V
Dissipated power	P_D	T_A = 25℃	-	500	-	mW
Ambient temperature	T_A	-	-40	-	125	℃

4.3.2.2 System Reset and Voltage Monitor

Table 4- 7 System and reset characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Band gap voltage	V_{BG}	-	-	1.2	-	V
Low power band gap Voltage	V_{LPBG}	-	-	1.1	-	V
Power on reset voltage	V_{POR}	0V up to VDDA, $T_{A=}$ -40~125°C	1.6	1.8	2.1	V
Power off reset voltage	V_{PDR}	Down to 0V, $T_{A=}$ -40~125°C	1.5	1.6	1.75	V
Reset delay time	t_{RSTPOR}	Power on reset	-	3	-	ms
	t_{RSTN}	External reset	-	5	-	us
Low voltage reset	V_{LVR}	LVRS=000	-	1.6	-	V
		LVRS=001	-	1.8	-	
		LVRS=010	-	2.0	-	
		LVRS =011	-	2.5	-	
		LVRS=100	-	2.8	-	
		LVRS=101	-	3.0	-	
		LVRS=110	-	3.5	-	
		LVRS=111	-	4.0	-	
LVR release hysteresis	$V_{HYS(LVR)}$	VDDA = 3.3V, T_A = 30°C	-	0.1	-	V
LVR working current	I_{LVR}	VDDA = 3.3V, T_A = 30°C	-	6	-	uA
LVD detection voltage	V_{LVD}	LVLS= 000	-	2.0	-	V
		LVLS = 001	-	2.2	-	
		LVLS = 010	-	2.4	-	
		LVLS = 011	-	2.7	-	
		LVLS = 100	-	2.9	-	
		LVLS = 101	-	3.1	-	

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
		LVLS = 110	-	3.6	-	
		LVLS = 111	-	4.5	-	
LVD release hysteresis	$V_{HYS(LVD)}$	VDDA = 3.3V, T_A = 30°C	-	0.1	-	V
LVD working current	I_{LVD}	VDDA = 3.3V, T_A = 30°C	-	6	-	uA

4.3.2.3 Internal Reference Voltage

Table 4- 8 Internal reference voltage characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Internal reference voltage	V_{REFINT}	$T_{A=}$ -40~125°C, VFS=0	-	1.6	-	V
		$T_{A=}$ -40~125°C, VFS=1	-	2.45	-	V
Distribution of the internal reference voltage within the temperature range	ΔV_{REFINT}	VDDA=3.3V, T=-40~125°C	-5	0	1	mV
Temperature coefficient	T_{coeff}	VDDA = 3.3V, T_A = 30°C	-	50	-	ppm/℃

4.3.2.4 Current Characteristics

The typical operating voltage of the device is 3.3V/5.0V. Here the values are tested with VDD=3.3V (T_A = 25℃) unless stated specifically.

Table 4- 9 Operating current characteristics

Parameter	Symbol	Peripheral status	Conditions	Min.	Typ. 3.3V	Typ. 5V	Max.	Unit
Operating current	I_{RUN}	Turn off	MCLK=8MHz, RCH/2	-	2.2	2.3	-	mA
			MCLK=16MHz, RCH	-	3.9	4.0	-	
			MCLK=24MHz, RCH+PLL ON	-	4.4	4.9	-	
			MCLK=48MHz, RCH+PLL ON	-	7.5	8.2	-	
			MCLK=72MHz, RCH+PLL ON	-	8.2	8.7	-	
			MCLK=96MHz, RCH+PLL ON	-	9.9	10.3	-	
			MCLK=108MHz, RCH+PLL ON	-	10.5	11.0	-	
		All turn on, ADC sampling turns on	MCLK=8MHz, RCH/2	-	5.8	6.6	-	
			MCLK=16MHz, RCH	-	7.7	8.5	-	
			MCLK=24MHz, RCH+PLL ON	-	8.2	9.3	-	
			MCLK=48MHz, RCH+PLL ON	-	8.4	9.7	-	
			MCLK=72MHz, RCH+PLL ON	-	11.3	12.6	-	
			MCLK=96MHz, RCH+PLL ON	-	13.0	14.3	-	
			MCLK=108MHz, RCH+PLL ON	-	15.2	16.3	-	
Sleeping current	I_{SLEEP}	Turn off	MCLK=8MHz, RCH/2	-	0.5	0.6	-	mA
			MCLK=16MHz, RCH	-	0.6	0.7	-	
			MCLK=24MHz, RCH+PLL ON	-	1.3	1.8	-	
			MCLK=48MHz, RCH+PLL ON	-	2.2	2.7	-	
			MCLK=72MHz, RCH+PLL ON	-	3.4	4.0	-	
			MCLK=96MHz, RCH+PLL ON	-	3.6	4.1	-	

Parameter	Symbol	Peripheral status	Conditions	Min.	Typ. 3.3V	Typ. 5V	Max.	Unit
			MCLK=108MHz, RCH+PLL ON	-	4.0	4.5	-	
		All turn on, ADC sampling turns on	MCLK=8MHz, RCH/2	-	3.8	4.5	-	
			MCLK=16MHz, RCH	-	4.5	4.9	-	
			MCLK=24MHz, RCH+PLL ON	-	5.6	6.5	-	
			MCLK=48MHz, RCH+PLL ON	-	7.5	8.7	-	
			MCLK=72MHz, RCH+PLL ON	-	10.5	11.5	-	
			MCLK=96MHz, RCH+PLL ON	-	12.0	12.7	-	
			MCLK=108MHz, RCH+PLL ON	-	13.0	13.6	-	

Note: *The following conditions apply to the measurement of current characteristics:*

** All IOs are set to output low and no load.*

** All modules have no load only with clock on unless specifically stated.*

Table 4- 10 Current consumption in Stop/ULP Stop modes

Parameter	Symbol	Conditions	Supply voltage	LDO Drive mode set to 50uA	Unit
Stop current (turn off all high frequency clocks and PLL)	I_{STOP}	All modules shut down	3.3V	55	uA
			5V	57	
		Only LVR and LVD turn on	3.3V	60	
			5V	63	
		Only WT turns on	3.3V	55	
			5V	58	
Parameter	**Symbol**	**Conditions**	**Supply voltage**	**Typ.**	**Unit**
ULP Stop Current (turn off all high frequency clocks and PLL, change to low power LDO)	$I_{ULTSTOP}$	All modules shut down	3.3V	7.0	uA
			5V	8.0	
		Only WT turns on	3.3V	7.1	
			5V	8.1	

4.3.2.5 Wake-up from Low Power Modes

Table 4- 11 Low power wake-up characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Wake-up time from Stop mode	t_{STOP}	-	100	-	us
Wake-up time from ULP Stop mode	$t_{ULTSTOP}$	-	240	-	

4.3.2.6 External Clock Characteristics

Table 4- 12 External clock characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
OSCL frequency	f_{OSCL_ext}	-	32.768	-	kHz
OSCL_IN input high voltage	V_{OSCLH}	-	0.5	-	V
OSCL_IN input low voltage	V_{OSCLL}	-	0	-	

Table 4- 13 External oscillator characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
OSCL current	I_{OSCL}	VDDH=3.3V, GAIN=00	-	0.70	-	uA
		VDDH=3.3V, GAIN=01	-	0.85	-	
		VDDH=3.3V, GAIN=10	-	1.25	-	
		VDDH=3.3V, GAIN=11	-	1.35	-	
OSCL set up time	$t_{SU(OSCL)}$	GAIN=00	-	0.25	-	s
		GAIN=01	-	0.15	-	
		GAIN=10	-	0.11	-	
		GAIN=11	-	0.15	-	

4.3.2.7 Internal Clock Characteristics

Table 4- 14 Internal clock characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RCH frequency	F_{RCH}	After calibration	-	16	-	MHz
RCH TRIM	$TRIM_{RCH}$	VDDH = 3.3V, T_A = 30°C	-	2	-	%
RCH duty cycle	$DuCy_{RCH}$	-	-	50	-	%
RCH accuracy	ACC_{RCH}	-	-	1	2.4	%
RCH set up time	$t_{SU(RCH)}$	-	-	6	-	us
RCH operating current	I_{RCH}	-	-	130	-	uA
RCL frequency	F_{RCL}	-	-	32	-	kHz
RCL TRIM	$TRIM_{RCL}$	VDDH = 3.3V, T_A = 30°C	-	0.8	-	%
RCL set up time	$DuCy_{RCL}$	-	-	50	-	%
RCL accuracy	ACC_{RCL}	-	-	-	10	%
RCL set up time	$t_{SU(RCL)}$	VDDH = 3.3V, T_A = 30°C	-	125	-	us
RCL operating current	I_{RCL}	VDDH = 3.3V, T_A = 30°C	-	300	-	nA

4.3.2.8 PLL Characteristics

Table 4- 15 PLL characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
PLL input frequency	f_{PLL_IN}	4	16	30	MHz
PLL input duty cycle	$DuCy_{PLL}$	30	50	70	%
PLL output frequency	f_{PLL_OUT}	30	108	256	MHz
PLL lock time	t_{LOCK}	-	5	14	us
PLL jitter	$Jitter_{PLL}$	-	13	40	ps

4.3.2.9 Flash Storage Characteristics

Table 4- 16 Flash storage characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Byte programming time	t_{prog}	-	-	-	8.5	us
Page erase time	t_{ERASE}	-	2	-	3	ms
Total erase time	t_{ME}	-	30	-	40	ms
Programming current	I_{prog}	-	-	0.5	0.8	mA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Erasing current	I_{ERASE}	-	-	-	0.8	mA
Endurance	N_{END}	-	100000	-	-	Cycles
Retention time	t_{RET}	T_A = 25°C	100	-	-	Years
		T_A = 85°C	20	-	-	

4.3.2.10 ESD Characteristics

Table 4- 17 ESD protection and latch-up characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
HBM	V_{HBM}	MIL-STD-883H	±4000	-	-	V
CDM	V_{CDM}	JESD22-C101E	±1000	-	-	
Latch-up trigger current	I_{LAT}	JEDEC standard NO.78D 2011.11	±200	-	-	mA
VDDH/VDDA over voltage	V_{LAT}		6.5	-	-	V

4.3.2.11 I/O Characteristics

Table 4- 18 I/O characteristics

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
IO input high voltage	V_{IH}	VDDH = 5V		-	2.0	-	V
		VDDH = 3.3V		-	1.5	-	
IO input low voltage	V_{IL}	VDDH = 5V		-	1.2	-	
		VDDH = 3.3V		-	1.0	-	
Input hysteresis	V_{HYS}	VDDH = 5V		-	0.5	-	V
		VDDH = 3.3V		-	0.4	-	
Output source current	I_{OH}	VDDH=3.3V V_{OH}=0.7*VDDH	Weak drive (DR=1)	-	20	-	mA
			Strong drive (DR=0)	-	40	-	
		VDDH=5V V_{OH}=0.7*VDDH	Weak drive (DR=1)	-	40	-	
			Strong drive (DR=0)	-	80	-	
Output sink current	I_{OL}	VDDH=3.3V V_{OL}=0.4V	Weak drive (DR=1)	-	10	-	mA
			Strong drive (DR=0)	-	20	-	
		VDDH=5V V_{OL}=0.6V	Weak drive (DR=1)	-	20	-	
			Strong drive (DR=0)	-	45	-	
IO input high current	I_{IH}	VDDH = 5V		-	-	0.1	uA
		VDDH = 3.3V					
IO input low current	I_{IL}	VDDH = 5V		-0.1	-	-	uA
		VDDH = 3.3V					
IO output high voltage	V_{OH}	VDDH = 5V	Strong drive I_{min}=16mA Weak drive I_{min}=8mA	4.5	-	-	V
		VDDH = 3.3V	Strong drive I_{min}=16mA Weak drive I_{min}=8mA	2.5	-	-	V
IO output low voltage	V_{OL}	VDDH = 5V	Strong drive I_{min}=16mA Weak drive I_{min}=8mA	-	-	0.3	V

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
		VDDH =3.3V	Strong drive I_{min}=16mA Weak drive I_{min}=8mA	-	-	0.4	V
Total output current	I_{total}	All ports		-	100	-	mA
Pull-up resistor	R_{pu}	V_{IN}=NULL		-	55	-	kΩ
Pull-down resistor	R_{pd}	V_{IN}=NULL		-	55	-	
Filter width	$T_{PW(IO)}$	External Reset pin		-	4	-	us
I/O capacitance	C_{IO}	-		-	-	10	pF

4.3.2.12 ADC Characteristics

Table 4- 19 ADC characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{adc}	V_{ref+}=4.9V(VFS=1)	4	-	5.5	V
		V_{ref+}=3.2V(VFS=0)	2.2	-	5.5	
Reference voltage	V_{ref+}	-	2	-	VDDA	V
Operating current	I_{ADC}	2MSPS (32MHz)[1]	-	3.5	-	mA
Operating frequency	f_{ADC}	-	0.1	-	32	MHz
Sampling rate	F_s	VDDA>4V	-	-	2	MSPS
		2.7V<VDDA<4V	-	-	1.5	
		2.2V<VDDA<2.7V	-	0.15	-	
Analog input voltage	V_{AIN}	VFS=1	0	-	4.9 or VDDA	V
		VFS=0	0	-	3.2 or VDDA	
Sampling switching resistor	R_{ADC}	-	-	1	-	kΩ
Internal sampling capacitor	C_{ADC}	-	-	1.2	-	pF
Latency of data preparation	$W_{LATENCY}$	-	-	2.5	-	$1/f_{pclk}$
Latency of trigger sampling	t_{latr}	-	-	2.5	-	$1/f_{ADC}$
Sampling time	t_{samp}	-	1	-	16	$1/f_{ADC}$
Conversion time	t_{conv}	-	13	-	16	$1/f_{ADC}$
Start-up time	t_{STAB}	-	32	-	512	$1/f_{ADC}$

Note: *The maximum operating frequency is 32MHz, and the corresponding sampling frequency can be up-to 2MSPS.*

Table 4- 20 VTS characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Linearity of V_{SENSE} with temperature	T_L	-	±4	-	°C
Average slope of temperature sensitivity Accuracy	Avg_slope	-	4.1	-	mV/°C
Sampling time of ADC getting temperature	t_{S_temp}	-	1	-	us
Voltage at 30°C(±5°C)	V_{30}	-	1.35	-	V

Table 4- 21 ADC Accuracy

Parameter	Symbol	Conditions	Typ.	Max.	Unit
Unadjusted total error	ET	-	+/-10	+/-40	LSB
Unadjusted offset error	EO	-	+/-5	+/-20	
Unadjusted gain error	EG	-	+/-5	+/-20	
Trim step size	-	-	0.8	-	

Parameter	Symbol	Conditions	Typ.	Max.	Unit
Trim range	-	-	-	+/-100	
Differential linearity error	ED	-	1	2	
Integral linearity error	EL	-	1	4	

4.3.2.13 OPA Characteristics

Table 4- 22 OPA characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{OPA}	-	1.8	3.3	5.5	V
Common mode input range	CMIR	-	0	-	VDDA	V
Input offset voltage	VI_{OFFSET}	No calibration, T_A = -40~125°C	-2.0	0	3.0	mV
		After calibration, T_A = -40~125°C	0.15	-	0.25	mV
Input offset voltage drift	ΔVI_{OFFSET}	-	-	0.05	-	uV/°C
Drive current	I_{LOAD}	-	-	5	-	mA
Dray current	I_{DD}	No load capacitance	-	80	-	uA
Common mode rejection ratio	CMRR	VDDA=3.3V, T_A = 30°C, C_L = 30pF	-	145	-	dB
Power supply rejection ratio	PSRR	VDDA=3.3V, T_A = 30°C, C_L = 30pF	-	130	-	dB
Bandwidth	GBW	VDDA=3.3V, T_A=30°C, offset current=4uA	-	10	-	MHz
Slew rate	SR	VDDA =5V, T_A = 30°C, C_L = 30pF	-	3.5	6	V/us
Resistive load	R_{LOAD}	-	0.1	10	-	kΩ
Capacitive load	C_{LOAD}	-	-	100	-	pF
High saturation voltage	VOH_{SAT}	-	-	3.8	-	mV
Low saturation voltage	VOL_{SAT}	-	-	3.3	-	mV
Phase margin	ϕm	VDDA=3.3V, T_A=30°C, C_L=50pF, offset current=4uA	-	25	-	°

4.3.2.14 ACMP Characteristics

Table 4- 23 ACMP characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{ACMP}	-	1.8	3.3	5	V
Input offset voltage	V_{os}	-	-	-	13	mV
Input common mode voltage	V_{cm}	Response time <160ns	0	-	VDDA	V
Compare hysteresis	V_{hyster}	-	-	20	-	mV
Transfer delay	T_{str}	CPDLY = 00, VDDA = 5V, FREN=0	-	40	-	ns
		CPDLY = 00, VDDA = 3.6V, FREN=0	-	50	-	
		CPDLY = 00, VDDA = 2.5V, FREN=0	-	60	-	
		CPDLY = 01, VDDA = 5V, FREN=0	-	120	-	
		CPDLY = 01, VDDA = 3.6V, FREN=0	-	145	-	
		CPDLY = 01, VDDA = 2.5V, FREN=0	-	200	-	

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
			CPDLY = 10, VDDA = 5V, FREN=0	-	320	-	
			CPDLY = 10, VDDA = 3.6V, FREN=0	-	450	-	ns
			CPDLY =10, VDDA = 2.5V, FREN=0	-	550	-	
			CPDLY = 11, VDDA = 5V, FREN=0	-	750	-	
			CPDLY = 11, VDDA = 3.6V, FREN=0	-	1000	-	
			CPDLY = 11, VDDA = 2.5V, FREN=0	-	1200	-	
Respons e time	Rising edge	T_{rt}	Normal response	-	50	-	ns
	Falling edge			-	55	-	
	Rising edge		Quick response	-	30	-	
	Falling edge			-	40	-	
Operating current		I_{cmp}	VDDA=5V, one channel of ACMP working	-	12	-	uA
Error offset ratio		dV_{offset}/dT	-	-	0.5	-	μV/°C

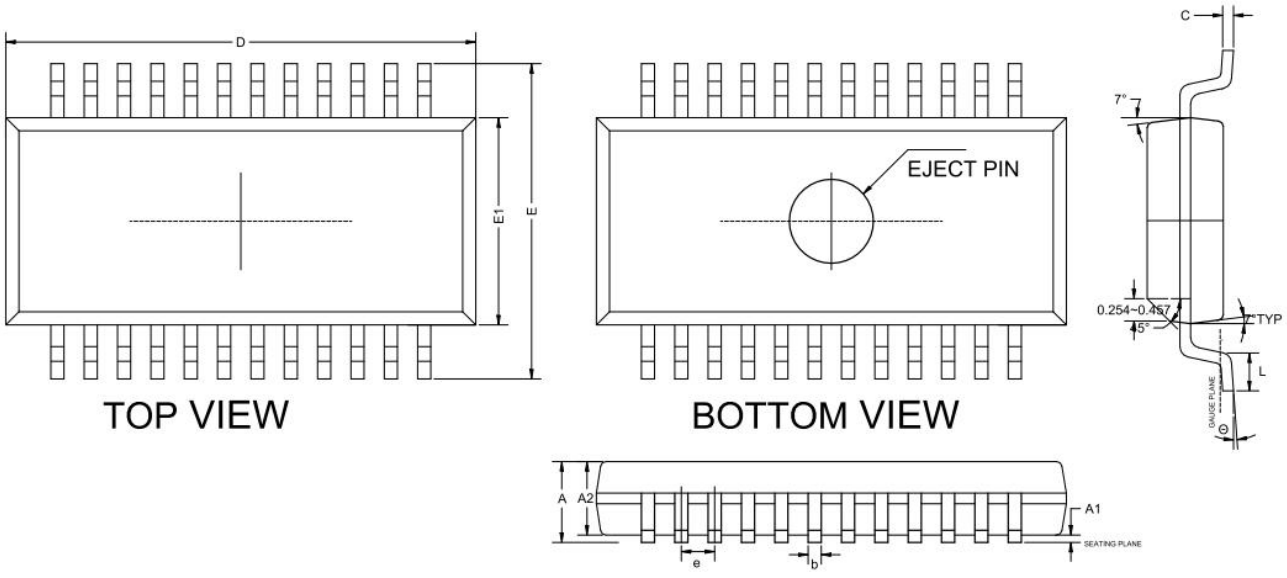
4.3.2.15 DAC Characteristics

Table 4- 24 DAC characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DAC}	-	1.8	3.3	5	V
Conversion time	t_{conv}	1LSB output variation, C_L=1pF	-	280	-	ns
Settling time	t_{settle}	VDDA = 3.3V, from 0V output to maximum full amplitude value, C_L=1pF	-	0.8	-	us
Output voltage	V_{OUT}	-	0.001	-	5.0	V
Operating current	I_{DAC}	-	-	200	-	uA
Resistive load	R_{load}	-	-	-	1	kΩ
Capacitive load	C_{load}	-	-	-	10	pF
Integral non-linearity error	INL	-	-	0.9	-	LSB
Differential non-linearity error	DNL	-	-	0.75	-	LSB
Offset error	Offset	-	-	1.5	-	mV
Gain error	Gain error	-	-	0.4	-	%
Time of WAKEUP	t_{WAKEUP}	-	-	5	-	us
Power supply rejection ratio	PSRR	Min. 1KHz, max. 1MHz	90	-	100	dB

5. Package Characteristics

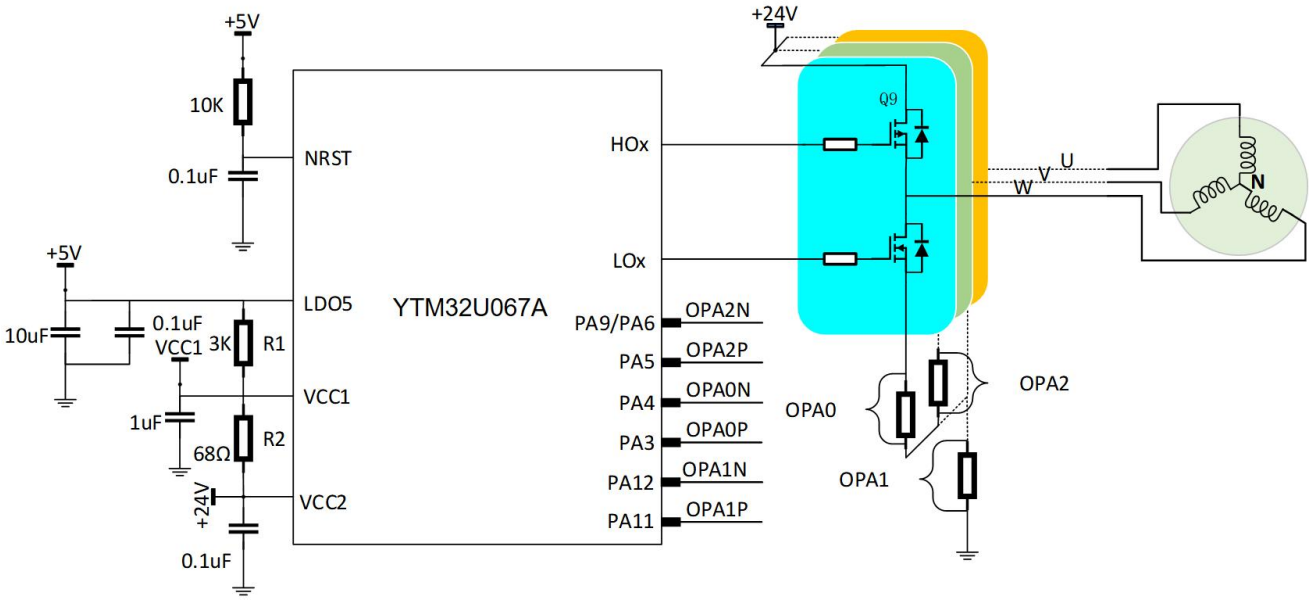
SSOP24 package outline



SYMBOL	MIN	NOM	MAX
A	1.50	-	1.75
A1	0.102	-	0.249
A2	1.40	-	1.55
D	8.582	-	8.738
E	5.842	-	6.198
E1	3.861	-	3.998
e	0.635BSC		
L	0.406	-	0.889
b	0.20	-	0.30
c	0.2TYP		
Θ	0°	-	8°

Figure 5- 1 Package information

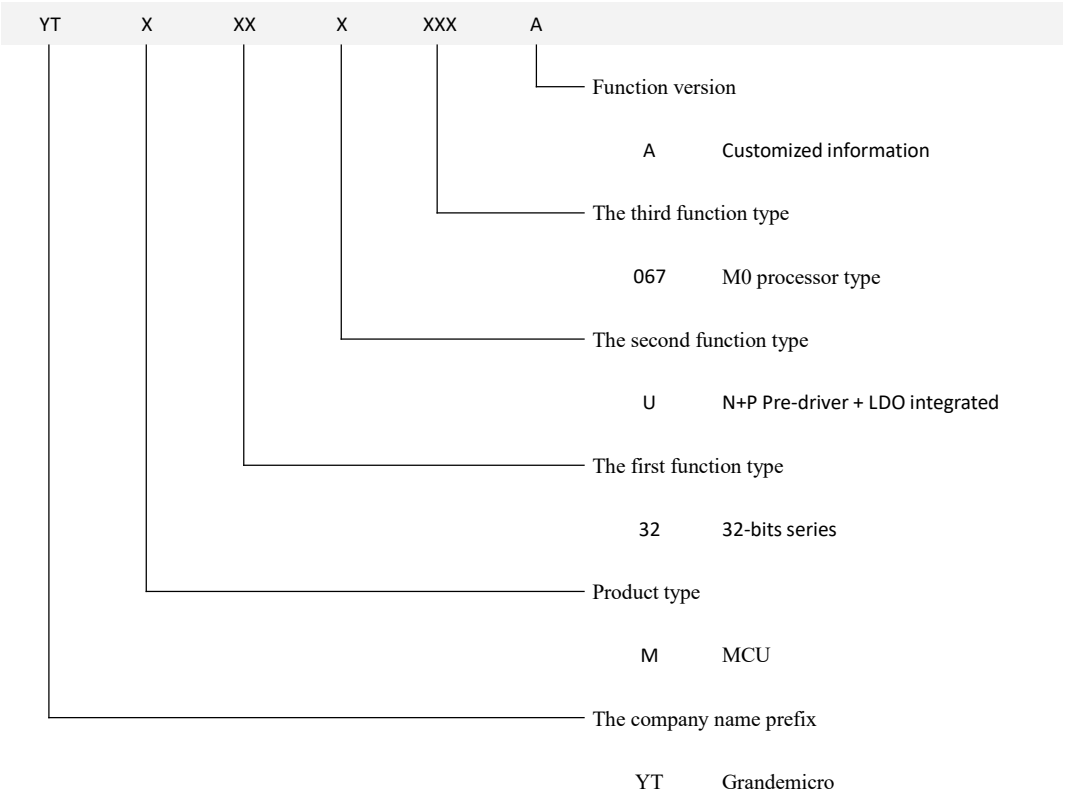
6. Application Circuit



Note: *Suitable for a wide voltage range, R1 can be removed and R2 can be increased within the normal voltage range. (VCC1 voltage is greater than 7V)*

Figure 6- 1 Typical application circuit

7. Marking Rule



8. Revision History

Table 8- 1 Revision history

Date	Rev.	Description of Change
2024.05.07	A0	First released
2024.09.02	A1	Adjust chip version
2024.10.08	A2	Correct clerical errors and adjust OPA characteristics
2025.03.01	A3	Product adjustment