433MHz Wireless Receiver Module

Features

- Work at 2.0V ~5.05V, with the power supply
- With high sensitivity (-110 dBm)
- Ultra-low startup time: 2.2ms, suitable for products with low power consumption requirements
- No external filter is required
- Consumption current is less than 3.3 mA
- The highest code rate is 8 kbps (no more than 3.5kbps is recommended)
- Consumption current is less than 0.1 μA in the energy-saving mode
- No register configuration required
- The SOP8 package of the chip was used
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Application

- Low-cost consumer electronics applications, such as remote control fans, remote control lights, remote control doors, remote control toys, etc
- Remote Key Entry System (RKE)
- Smart home, building monitoring automation
- Wireless doorbell and remote RFID
- Industrial inspection and control system
- Other one-way RF receiving application areas

Functional Block Diagram

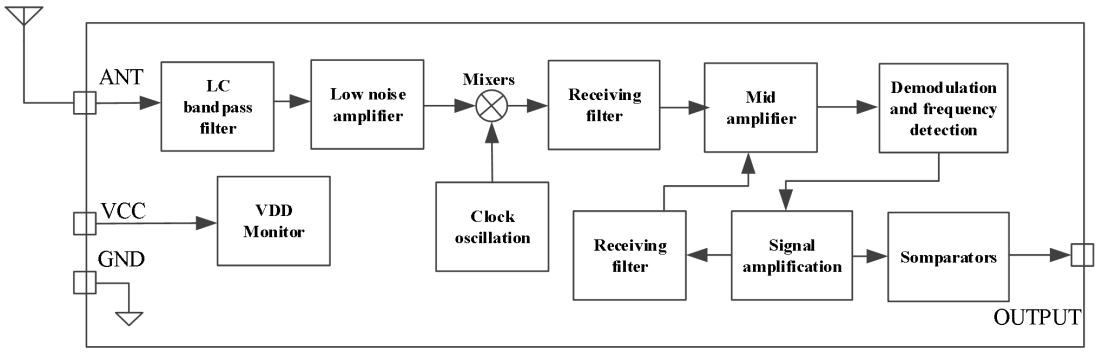

Fig. 1. Functional block diagram

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Ordering Information

Part No.	Type	Size	Operating Temperature	Packing Method
YT520MA	Module	16.9mm*10.77mm	-40℃ to 85℃	50pcs/Bag

Package the Physical Pin Definition

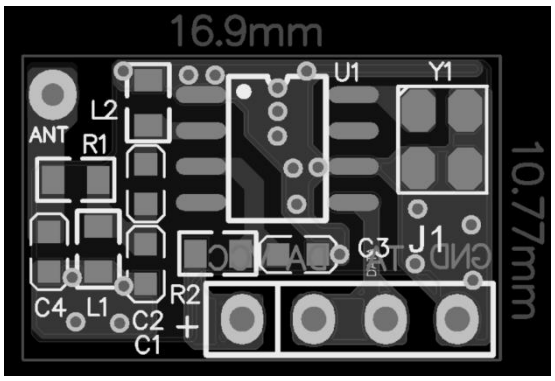

Fig. 2.Physical PCB size

Fig. 3.Physical pin definition

Pin Definition

Pin No.	Name	Description
1	VCC	Positive power input
2, 3	DATA	Signal output
4	GND	Negative power input
/	ANT	Antennae
Pin Header		Pin-row_R1 type_Pitch :2.54mm_1x4p_Bent insert_Policy_ Single row_Plastic height 2.5mm_Lower pin C6.0mm_Upper pin D3.0mm_Black_94-V0
ANT Wire		Spring wire_Black Rubber Spiral Shape_10 turns_Wire Diameter Outer diameter ¢1.05mm_One end stripped 3mm_the other end not stripped_433MHz_Copper

Typical Application Circuit[Note1]

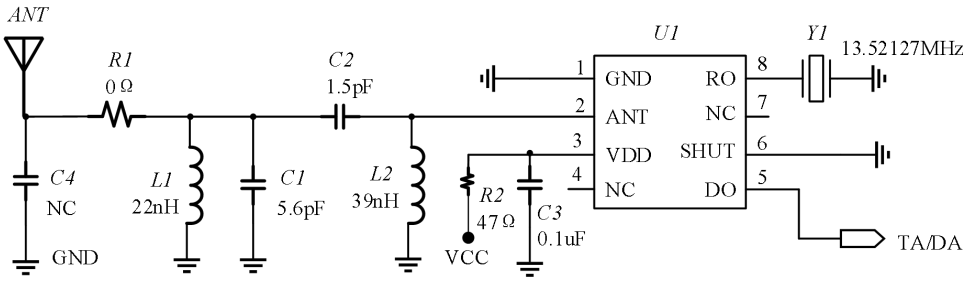

Fig. 4.Typical application circuit

Note1: In order to ensure that the voltage supplied to the chip does not exceed the maximum operating voltage of the chip, 22~51Ohm resistance should be added to the power supply when applying 5V. Add the resistance after the formation of RC filtering, but also can make the product better resist the power surge, spike, burr and other abnormal conditions.

Absolute Maximum Ratings[Note2]

Parameters	Symbol	Range	Units
Supply Voltage of VCC	V_{CC}	-0.3~5.5	*V*
"ANT", "DA" and "TA" Voltage range	V_{ANT},V_{DA} *and* V_{TA}	-0.3~VDD+0.3	*V*
Maximum input power	P_{INMAX}	10	*dBm*
Lead Weld Resistance Temperature (welding, 10s)	T_{lead}	255	℃
Storage Temperature	T_{stg}	-65~150	℃
Junction Temperature	T_j	150	℃

Note2：All voltages are GND and exceeding the absolute maximum rating may cause device damage.

Recommended Working Conditions[Note3]

Parameters	Symbol	Range	Units
Supply Voltage of VCC	V_{CC}	2.0~5.05	*V*
"ANT", "DA" and "TA" Voltage range	V_{ANT},V_{DA} *and* V_{TA}	0.3~VDD+0.3	*V*
Maximum input power	P_{INMAX}	0	*dBm*
Modulation Duty Cycle	D_M	20~80%	/
RF Code Rate	R_C	2	*kbps*
Frequency Range	F_Q	*433MHz±0.3*	*MHz*

Note3：Beyond the range of recommended working conditions. Unless otherwise specified, the test conditions are as follows: VCC= 5V ,TA =25℃.

Receiver Specification[Note4] (Unless otherwise specified, T_a = 25 ℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
VCC	Power Supply Voltage		2.0		5.05	V
f_{RF}	Operating Frequency Range	f_{RF}=13.52127 MHz		433.92		MHz
DR	Data Rate		0.1		3.5	kbps
I_{OP}	Operating Current	f_{RF}=433.92MHz,VDD=3.3V		3.0		mA
		f_{RF}=433.92MHz,VDD=5V		3.17		mA
I_{STBY}	Sleep Current	VSHUT=VDD		0.01		μA
S_{433}	Receiving Sensitivity	f_{RF}=433 .92MHz		- 110		dBm
f_{BW}	Receiver Bandwidth	f_{RF}=433 .92MHz		250		kHz
f_{IF}	Intermediate Frequency			0.86		MHz
f_{BW}	Intermediate Frequency Bandwidth			0.43		MHz
	Saturated Input Level	RSC=50 Ω		-20		dBm
	Spurious Reverse Isolation	ANT pin, RSC= 50 Ω		30		μVr/ms
ZREFOSC	Reference oscillator Input Impedance			290		kΩ
I_{ROSC}	Reference oscillator source current			5.2		μA
f_T	Crystal Oscillator Frequency	f_{RF}=433.92MHz		13.52127		MHz
T_{RST}	Receiver Startup Time	From the power-on of VDD to reception		3		ms
T_{SST}	SHUT Startup Time	From pulling the SHUT pin low to reception		2.2		ms

Note4：The max and minimum parameters specified are guaranteed by test, the typical value are guaranteed by design, characterization and statistical analysis.

Functional Description

The YT520MA module wireless receiver is used in 433MHz low-power, low-cost short-distance front end, with high sensitivity (-110 dBm), low power performance (<3.3 mA), and a high dynamic range (more than 60dB). The complete RF front-end, IF filter and ASK / OOK simulation demodulation part are integrated, with a high degree of integration.

Receiver Channel

The YT520MA series of short-range wireless communication receivers are highly integrated with a complete RF front-end and ASK/OOK analogue demodulation. The RF front-end consists of a low noise amplifier, mixer, mirror rejection filter, variable gain amplifier and frequency synthesizer; the ASK/OOK analogue demodulation consists of a low-pass filter, automatic gain control circuit, signal amplitude indication circuit, limiting amplifier and squelch circuit.

Low-noise Amplifier, Mixer

The low noise amplifier adopts a common source common gate structure, and the output signal is changed into two circuits through a single circuit structure (STD), which is provided to the latter level mixer. The mixer adopts the Gilbert double balanced mixer structure, and its gain is controlled by the AGC circuit.

Filter and Tuning Circuit

The MF filter tuning circuit is based on the VCO type phase-locking loop, whose VCO consists of the filter component unit composed of GmC. The pressure-controlled oscillator (VCO) and the span guide amplifier in the complex filter match, and the capacitance match. The oscillation signal generated by VCO locks the frequency at the reference frequency by the phase-locking ring (PLL), and determines the integration time constant of each integrator in the filter, so as to realize the control of the transmission function of the filter and achieve the purpose of tuning the filter.

The ASK / OOK Demodulation Circuit

The demodulation circuit is mainly composed of: peak detector, programmable filter, integrator, signal flipper and demodulator control module.The peak detector detects the IF differential signal of the front and continuously charges and discharges the load capacitance so that the voltage of the load capacitor is equal to the peak voltage of the difference signal.The programmable filter internally uses the switching capacitor filter circuit to filter the signal, and filter out the signal harmonic noise component to get the analog signal we need. The automatic gain control module can timely adjust the gain of the variable gain amplifier in the forward signal path according to the analog signal swing to stabilize the voltage swing of the signal.The signal flip device adopts a feedback structure to shorten the flip time, and adds the output buffer level to improve the driving load capacity. Once this simulation exceeds the threshold, the output of the signal flip apparatus is a "1" signal, or otherwise a "0" signal instead.

Phase-locked ring circuit

The phase-locked loop circuit PLL provides the local signal for the reception, and the operating frequency points are 433MHz. In order to realize low power consumption, the local vibration signal provided by the ring oscillator is adopted, and the fixed 32 frequency division is adopted in the loop to simplify the charge pump structure and build the loop filter. The third-order loop filter structure is adopted, and the second-order output in the loop filter serves as the signal of the filter bandwidth adjustment, and the power consumption of the overall PCL circuit is below 1mA.

Stabilized voltage supply

Internal integrated regulator power supply circuit (LDO). In the voltage change of external power supply or surge burr, the voltage power supply circuit can still provide stable power supply voltage for the internal module circuit, improve the stability and reliability of the circuit in various application environments, and reduce the use cost of users.

Matters need attention

The product is a CMOS device, so attention should be paid to anti-static during storage, transport and use.

The device should be well grounded when in use.

RF devices are voltage sensitive devices, if the power supply is unstable or ripple is large, please add filtering to the power input to ensure that the supply voltage does not exceed the maximum operating voltage of the product.

Version History

Version	Date	Description
A0	Mar. 2025	Draft
A1	Jun. 2025	Released