YT91021NH8

Constant Voltage PSR Regulator with Active Power Factor Correction

Features

- High Precision (±3%) Constant Voltage Regulation
- Primary Side Regulation Technology
- Constant On Time Control for Active PFC with High Power Factor (>0.9) and Low THD (<10%)
- Audio Noise Free Operation
- Independent HV Pin for Start-up
- Real Time Digital Compensating Technology for Excellent Line and Load Regulation
- Quasi-resonant Operation with Frequency Clamping for High Efficiency and Low EMI Operation
- Integrated 1kV SiC MOSFET
- HSOP8 Package

Protection

- Built-In Soft Start
- Output Open Protection
- Output Short (SCP)
- Over Temperature Protection (OTP)
- Over Load Protection (OLP)
- Line Under Voltage and Over Voltage Protection
- Cycle-by-Cycle Current Limiting
- Leading Edge Blanking for Current Sensing
- VCC Under Voltage Lock Out (UVLO)
- VCC Over Voltage Protection (VCC OVP)

Application

- AC-DC Adapter with PFC Function

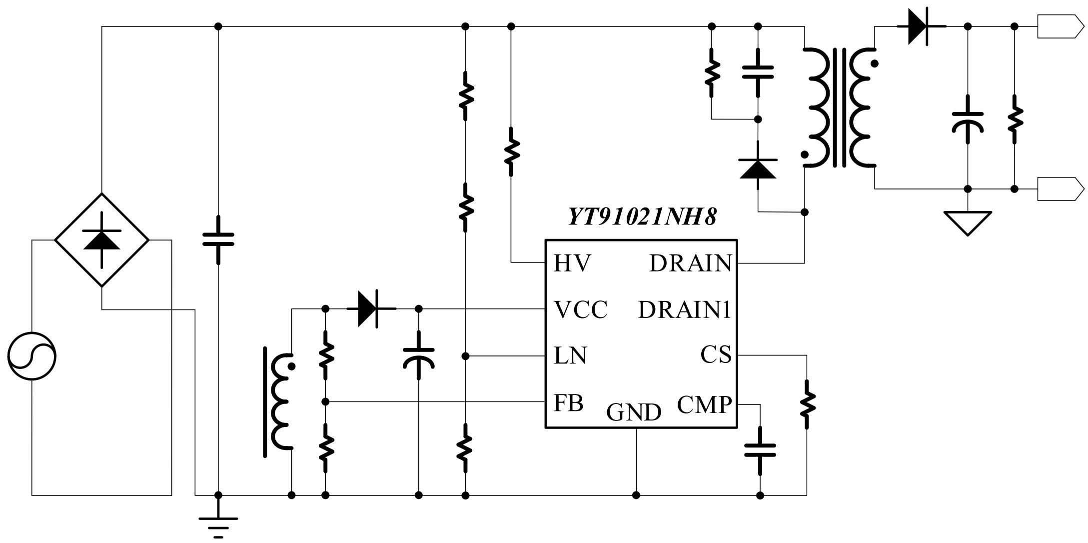

Fig. 1. Typical application circuit

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Package and Ordering Information

Part No.	Material Type	Package	Operating Temperature	Built-in MOSFET	Packing Method
YT91021NH8	Green	HSOP8	–40°C to 105°C	1kV 0.48ohm	Tape 5000 pcs/Reel

Pin Configuration

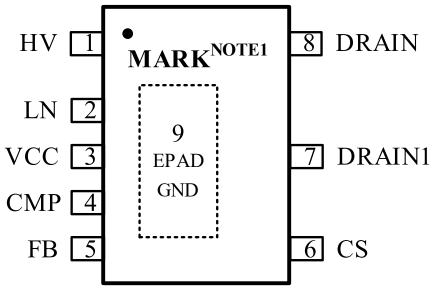


Fig. 2. Pin configuration

Note 1: Please refer to the "Marking Rule".

Pin Definition

Pin No.	Name	Description
1	HV	High voltage pin for start-up A resistor larger than 100kohm should be connected between the bulky capacitor and this pin to withstand surge
2	LN	Line voltage detection and protection with adjusted resistor LN cannot be floated, and its voltage level should be within 1.15V to 3.4V to avoid protection
3	VCC	Power supply buffer for chip
4	CMP	Output of the internal OTA. Connect it to a proper compensator network
5	FB	Voltage feedback from auxiliary winding with voltage divider for output voltage control
6	CS	Current sense for maximum loading setting with resistors connected to GND
7	DRAIN1	The drain of the internal low voltage silicon MOS and same as source of the SiC MOS No external connection is required
8	DRAIN	Drain of the integrated high voltage MOSFET
9/EPAD	GND	Ground

Internal Block Diagram

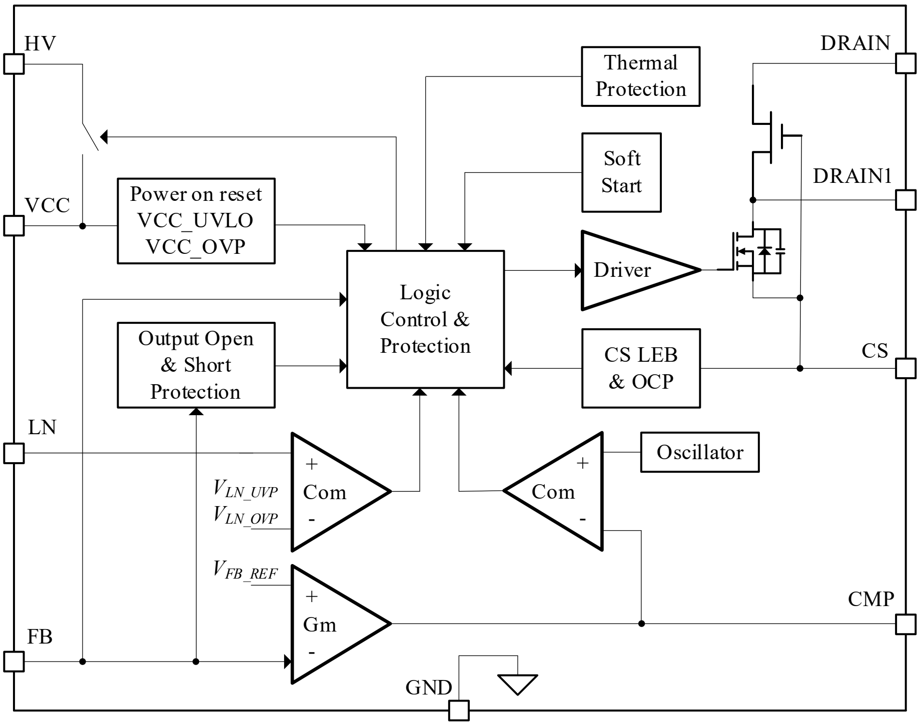


Fig. 3 Internal block diagram

Absolute Maximum Ratings[Note2]

Parameters	Symbol	Range	Units
"HV" voltage range	V_{HV}	– 0.3 ~ 600	V
"VCC" voltage range	V_{VCC}	– 0.3 ~ 45	V
"CS", "LN", "FB", "CMP" voltage range	V_{CS}, V_{LN}, V_{FB}, V_{CMP}	– 0.3 ~ 7	V
Guaranteed minimum "DRAIN" voltage[Note3]	V_{DS_min}	1000	V
Guaranteed minimum "DRAIN1" voltage[Note3]	V_{DS1_min}	30	V
ESD Human mode[Note4]	ESD_{hbm}	2000	V
Operating junction temperature range	T_j	– 40 ~ 150	°C
Ambient temperature range	T_a	– 40 ~ 105	°C
Storage Temperature Range	T_{stg}	– 65 ~ 150	°C
Welding temperature (< 20s welding)	T_{lead}	260	°C
Junction to ambient thermal resistance	θ_{thja}	45	°C/W

Note 2: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

Note 3: Depending on the different built-in MOSFET SPEC, see the corresponding relationship between the model and the built-in MOSFET.

Note 4: Electrical components and circuit boards will be aware of the situation in the discharge is not easy. Although this product has a special electrostatic protection circuit, but in the case of high-energy electrostatic discharge, the chip may have damage and loss of function or performance degradation. Therefore, users still need to take appropriate preventive measures ESD.

Electrical Characteristics[Note5] (Unless otherwise specified, T_a = 25 ℃)

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
HV						
Output Voltage to VCC	V_{HV_VCC}	HV = 140V	27		30	V
Output Current to VCC	I_{HV_VCC}			3		mA
Leakage Current	I_{HV_DSS}	HV = 600V			10	µA
VCC						
VCC Start-up Current	I_{ST}	$V_{VCC} = V_{UVLO\_OFF} - 1V$	3	7	20	µA
VCC Operation Current	I_{OP}	V_{VCC} = 20V	0.8	1	1.4	mA
VCC Under Voltage Lock Out Enter	V_{UVLO_ON}	V_{VCC} Falling	5.8	6.8	7.8	V
VCC Under Voltage Lock Out Exit	V_{UVLO_OFF}	V_{VCC} Rising	20	22.5	25	V
VCC Over Voltage Protection	V_{VCC_OVP}		29	32	35	V
PWM						
Maximum On Time	T_{on_max}			22		µs
Maximum Off Time	T_{off_max}			75		µs
Maximum Frequency	f_{max}			100		kHz
Minimum Frequency	F_{min}			500		Hz
CS						
CS Sampling OCP Voltage	V_{CS_OCP}	T_{ON} = 0 µs		0.7		V
CS Leading Edge Blanking Time	T_{LEB_CS}			300		ns
FB						
Reference Voltage	V_{FB_REF}		2.42	2.5	2.58	V
Output OVP Threshold	V_{OVP_FB}		3.1	3.2	3.3	V
FB Short Protection	V_{SCP_FB}			0.4		V
LN						
AC Line UVP Threshold	V_{LN_UVP}		0.85	1	1.15	V
AC Line OVP Threshold	V_{LN_OVP}		3.4	3.55	3.7	
Hysteresis for UVP	V_{hys_UVP}		5	15	25	
Hysteresis for OVP	V_{hys_OVP}		25	35	45	V
Gm Amplifier (OTA)						
Transconductance Gain	Gm			40		µS
MOS						
Drain-Source Breakdown Voltage	BV_{DSS}	Drain to source voltage @V_{GS}= –30V	1000			V
Drain-Source On Resistance	R_{DS_ON}	V_{GS}=12V，I_D=2A，T_J=25°C		0.48		ohm
OTP						
OTP Threshold	T_{OTP}			150		℃

Note 5: The max and minimum parameters specified are guaranteed by test. The typical values are guaranteed by design, characterization and statistical analysis.

Application Suggestion

YT91021NH8 is a high precision active PFC regulator, specially designed for PSR flyback offline constant voltage control. Operating in critical conduction mode with quasi-resonant to achieve high power factor, low THD and high efficiency.

HV Start Up

HV start-up technology is used in the chip to meet the fast start-up time requirement. Meanwhile, low I_{ST} is designed for VCC so that it can be charged above V_{UVLO_OFF} with small current.

During the start-up, the capacitor voltage at CMP is pulled up quickly. The chip operates at short-circuit mode and over current protection is set cycle-by-cycle until it senses the output voltage by FB above 1.3V. After that, the chip operates in close loop.

Loop Compensation

Output voltage is feedback to FB from the voltage divider with the auxiliary winding and compared with an internal reference (2.5V) at the positive input of the operational transconductance amplifier (OTA) for regulation.

The output of the OTA is the CMP which can be compensated externally with a capacitor for loop stability. The system bandwidth shall be set below 20Hz to suppress the AC ripple of the line.

Constant Voltage Control

The chip samples the output voltage through the auxiliary winding, divides the voltage and compares it with the internal reference to form a closed loop, and then keeps the output voltage constant. The output voltage formula is:

$$V_{out} = V_{FB\_REF} \times \frac{(R_{FBL} + R_{FBH})}{R_{FBL}} \times \frac{N_{sec}}{N_{aux}} - V_{SD} \qquad (1)$$

Where R_{FBL} is FB pull-down resistance, R_{FBH} is FB pull-up resistance, N_{aux} is the turns of the auxiliary winding, and V_{SD} is the voltage drop of rectifier diode on the secondary side. At the zero-crossing point of the secondary current, V_{SD} is almost equal to zero and can be neglected.

Active Power Factor Correction (APFC)

The duration of the turn on period (T_{on}) is generated by comparing an internal fixed saw-tooth wave with the voltage on the CMP pin. During steady state, the voltage on CMP pin is slowly varying due to the large external capacitor, therefor the T_{on} can be considered constant. In flyback operation, constant T_{on} and quasi-resonant operation provide input current shaping as sinusoidal as shown in Fig. 4 and achieving active power factor correction, thereby high power factor and low THD can be expected.

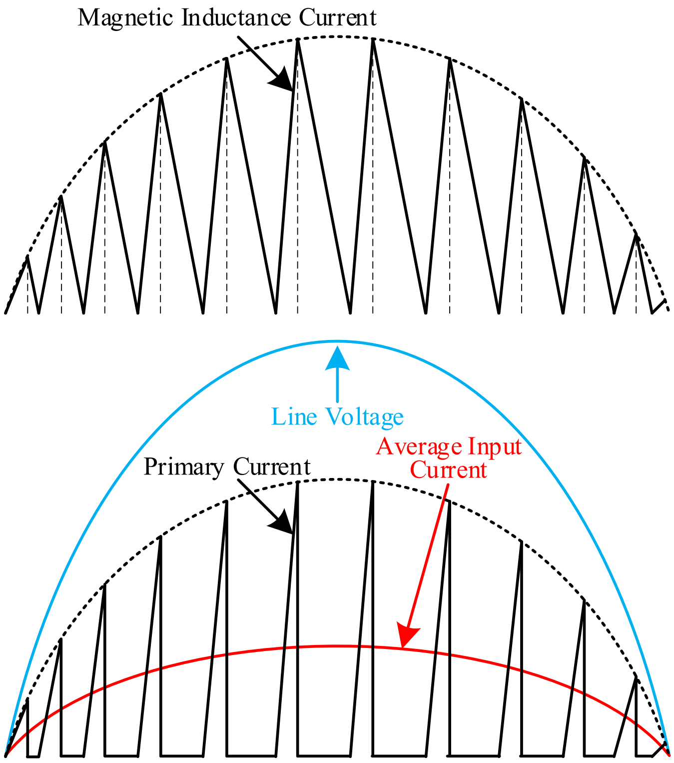


Fig. 4 Key waveforms of the constant T_{on} controlled flyback with APFC

Quasi-resonant Operation

Dedicated zero crossing detection of the inductor current is designed for PWM turn-on signal, thereby the valley turn-on of the MOSFET and quasi-resonant operation can be achieved.

ZCD Blanking

Fig. 5 shows ZCD blanking time (T_{LEB_ZCD}) is set to avoid the fault trigger by the oscillation after the turn off.

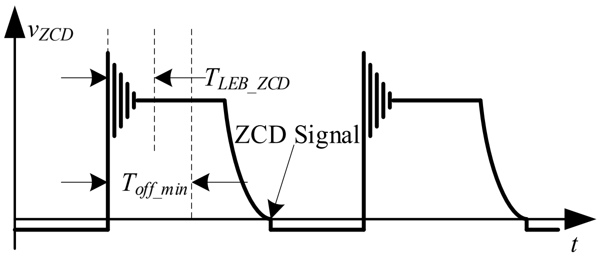


Fig. 5 ZCD blanking

Maximum Frequency Setting

Minimum off time (T_{off_min}) is set to limit the maximum switching frequency (f_{sw_max}), then the switching loss and EMC performance can be guaranteed. As shown in Fig. 6, PWM is triggered at the first valley after T_{off_min}.

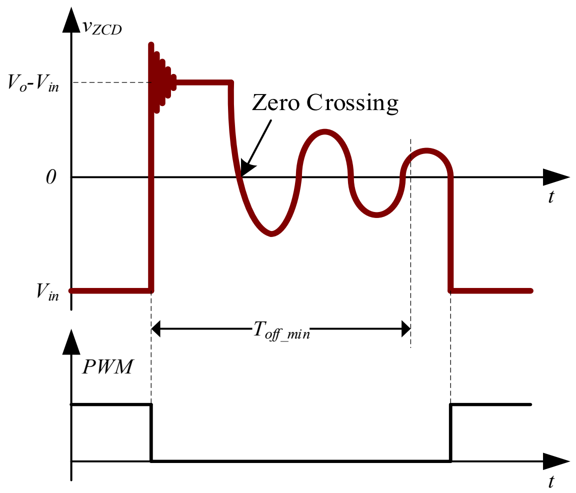


Fig. 6 Minimum off time

CS Blanking

Fig. 7 shows CS blanking time (T_{LEB_CS}) is set to avoid the fault trigger by the noise after the turn-on.

Cycle by Cycle Current Limiting

When magnetic inductance saturation happens, CS pin voltage (V_{CS}) goes higher than regulation. However, CS voltage limit (V_{CS_OCP}) can help to stop PWM cycle by cycle to protect the MOSFET and the other power devices.

Short Circuit Protection (SCP)

When output is short, the FB voltage is low. If the voltage at FB pin is lower than FB short protection threshold V_{SCP_FB}, then the CS sampling OCP voltage V_{CS_OCP} is reduced to 0.4V (typical) to reduce the dissipation of the power.

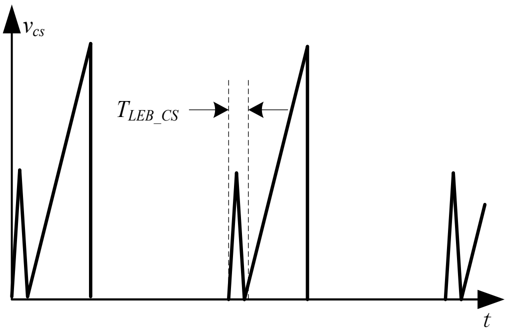


Fig. 7 CS blanking

Over Voltage Protection for Output

When the platform voltage detected by FB reaches the internal open circuit protection threshold V_{OVP_FB}, the system enters open circuit protection, the chip shuts down and enters into power on start-up sequence thereafter. The open circuit protection voltage is:

$$V_{OVP} = V_{OVP\_FB} \times \frac{(R_{FBL} + R_{FBH})}{R_{FBL}} \times \frac{N_{\sec}}{N_{aux}} - V_{SD} \qquad (2)$$

Where V_{OVP} is the over voltage protection point that needs to be set.

Over Load Protection (OLP)

Chip detects the output power and offers over load protection (OLP). If output power exceeds the power limit threshold (typical 1.3 times the full load), the chip reacts to turn off the power MOSFET. After 150ms (typical), the OLP stave can be reset.

Over Temperature Protection (OTP)

When the junction temperature goes higher than the OTP Threshold, chip shuts down and keep the state until a new restart.

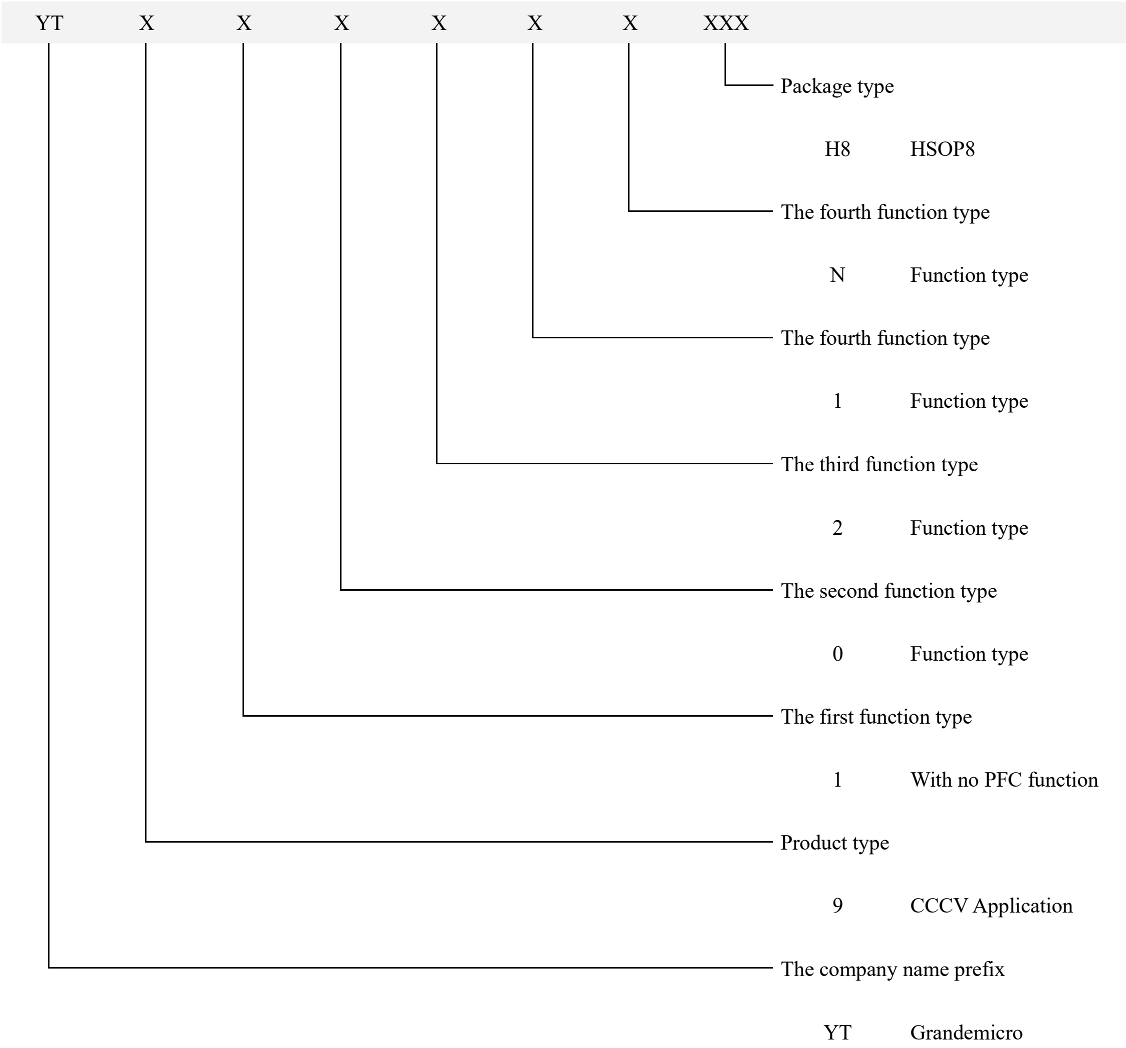
LN Protection

LN pin detects the line voltage through the voltage divider which is connected as shown in Fig. 1. User can program the over voltage protection threshold and the over voltage protection threshold by configuring the voltage divider network. 3.9kohm is recommended for the bottom LN detection resistor R_{LNL}. LN cannot be floated. Users need to correctly set the LN voltage level between 1.15V and 3.4V.

PCB Design Guide

1. Current sensing resistor (R_{cs}) shall be placed very close to the chip, minimize the loop from CS pin to R_{cs} and GND pin.
2. Separate the power ground and the signal ground. Please use star connection method to connect power ground, signal ground to GND pin.
3. Keep DRAIN1 floated without any connection.
4. The R_{LNL} resistor should be placed close to the LN pin of the chip, and a 10nF filter capacitor should also be added.

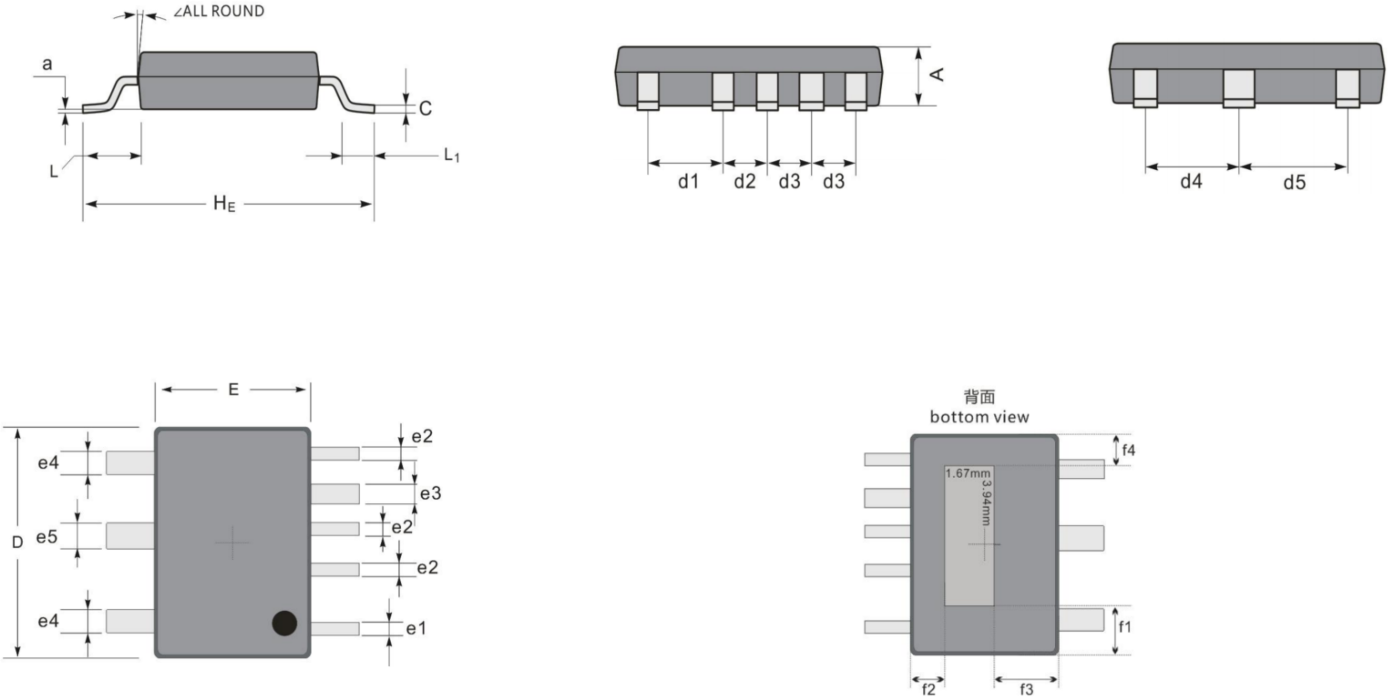
Marking Rule



●	Part No. Date Code Special Note
Part No.	YT91021N
Date Code	P: Packing site; Y: Year; W: Week; S: Series; V: Version.
Special Note	Use obvious mark like “H”, “L” to distinguish the key features like CS or FB reference etc. if necessary.
●	The first pin marked

Package

HSOP8



Unit		A	C	D	E	HE	d1	d2	d3	d4	d5	e1	e2	e3	e4	e5	L	L1	f1	f2	f3	f4	a	∠
mm	max	1.25	0.22	6.4	4.1	6.1	2.38	1.00	1.05	2.30	2.80	0.40	0.35	0.45	0.65	0.85	1.15	0.80	1.65	0.85	1.48	0.71	0.2 (ref)	12°
	typ	1.15	0.20	6.2	3.9	6.0	2.33	0.95	1.00	2.25	2.75	0.35	0.30	0.40	0.60	0.80	1.05	/	1.6	0.8	1.43	0.66		
	min	1.05	0.15	6.0	3.7	5.9	2.28	0.90	0.95	2.20	2.70	0.30	0.25	0.35	0.55	0.75	0.95	0.40	1.55	0.75	1.38	0.61		
mil	max	49	9	252	161	240	94	39	41	91	110	16	14	18	26	33	45	31	65	33	58	28	8 (ref)	
	typ	45	8	244	154	236	92	37	39	89	108	14	12	16	24	31	41	/	63	31	56	26		
	min	41	6	236	146	232	90	35	37	87	106	12	10	14	22	30	37	16	61	30	54	24		

Version History

Version	Date	Description
A0	Nov.2025	Draft
A1	Dec.2025	Released