32-bit CPU, 64kB Flash/10kB RAM, up to 25 fast I/O, 7 Timers,
4 Communication interfaces supporting LIN, 1 ADC, 1 DAC, 2 ACMPs, 3 OPAs, 2.0~5.5V

Features

- **108MHz 32–bit M0 core**
  - CORDIC co–processor
  - Hardware divider
  - CRC unit
  - Industrial–grade operating temperature
- **Built-in MOSFET and drive characteristics**
  - Integrated gate drive circuit and 3 pairs of P+N MOS, with a continuous over–current capacity of 6A
  - Wide input voltage range: 6.5V to 40V
  - Maximum Output Frequency 50kHz
  - P+N RDSON: typical value is 40.6mΩ at VGS=10V
  - Junction temperature from –40°C to 125°C
- **Built-in LDO**
  - Typical output voltage is 5V, and supporting a load capacity of up to 50mA.
- **Memories**
  - 64Kbytes Embedded Flash (32–bit width), supporting prefetch and read/write protection, supporting parity check
  - 10kbytes SRAM (32-bit width) divided into two independent partitions of 4kbytes and 6kbytes, and supporting parity check
  - 16KBytes ROM, supporting boot from ROM and secure fault handling
- **Reset and power management**
  - 2.0V to 5.5V power supply and I/O
  - Embedded two LDOs: normal LDO and low–power LDO
  - High–precision power–on & power–down reset (POR_PDR)
  - Low–voltage reset circuit (LVR): 8 reset points are available (1.6V, 1.8V, 2.0V, 2.5V, 2.8V, 3.0V, 3.5V, 4.0V)
  - Low-voltage detection circuit (LVD): 8 detection points are available (2.0V, 2.2V, 2.4V, 2.7V, 2.9V, 3.1V, 3.6V, 4.5V)
- **Clock System**
  - Built–in factory–calibrated 16MHz RC oscillator (RCH, 1% accuracy)
  - 32KHz low-speed oscillator crystal (OSCL)
  - Built–in factory–calibrated 32KHz RC oscillator (RCL, 10% accuracy)
  - Internal PLL up to 256 MHz with jitter less than 100ps
- **Low power**
  - Three low–power modes: sleep, stop, and ultra–stop modes
- **Debug mode**
  - Serial wire debug port (SW-DP)
- **Boot modes**
  - Boot from Flash or SRAM
- **Programming modes**
  - In-Circuit Serial Programming (ISP)
- **Peripherals**
  - Two UART
  - One SPI
  - One I2C
  - One 16–bit advanced–control timer TIM1
  - Four 16–bit general–purpose timers TIM2, TIM15, TIM16, TIM17
  - One independent window watchdog timer
  - One 24–bit down–counter SysTick timer
  - One watch timer
  - Up to 11 fast I/O ports
- **Analog modules**
  - One 12–bit A/D converter One SPI
  - One 10–bit D/A converter
  - Two analog comparators (ACMP)
  - Three operational amplifiers (OPA)
- **Built-in under-voltage, over-current, and over-temperature protection**
  - Under-voltage protection (UVP): 4.5V
  - Over-current protection (OCP): according to customer requirements
  - Over-temperature protection (OTP): trigger point is 150°C, recovery temperature is 135°C

Address: Room 1501, Block A3, West Jianzhu Rd. 777, Binhu District, Wuxi, Jiangsu , China
Phone/Fax: 86-510-85388846

1. Overview

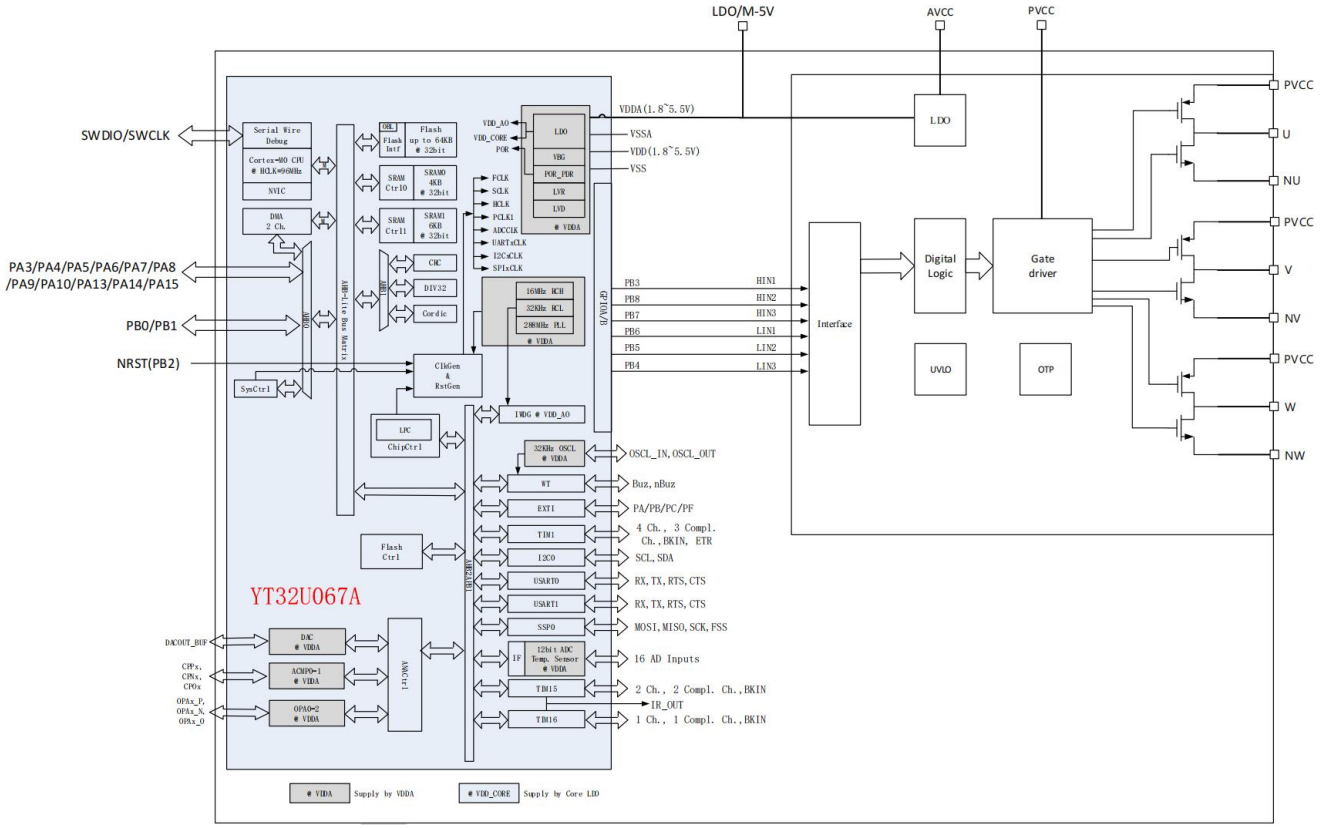
The YTM32M067AS21 series is a highly integrated three–phase motor driver IC designed for high–efficiency motor control applications. The chip integrates an LDO voltage regulator, over–temperature protection (OTP), and multiple protection mechanisms, supporting flexible configuration and low–power modes. With an operating voltage range from 5V to 28V, it features a stable LDO 5V output with a current capacity of up to 50mA.

This series demonstrates robust driving performance, supporting continuous drive currents up to 6A. The exceptionally low combined on–resistance of its PMOS and NMOS transistors effectively minimizes power dissipation and reduces heat generation, making it ideal for motor applications below 36W.

The YTM32M067AS21 series incorporates advanced protection features including over–current protection (OCP), under–voltage protection (UVP),and over–temperature protection (OTP), ensuring system stability under harsh operating conditions. This solution is widely adopted in industrial fans,consumer–grade motor applications, and other motor–driven systems requiring reliable performance.

Model	Operating Voltage	Package	Built-in MOS	Total On-Resistance @Vgs=10V	Maximum Phase Current (Peak-to-Peak)	Continuous Current	Number of Available I/O
YTM32M067AS21	5~28V	SSOP21	✓	40.6mΩ	6A	4.0A	11

2. Function Diagram



3. Memory Mapping

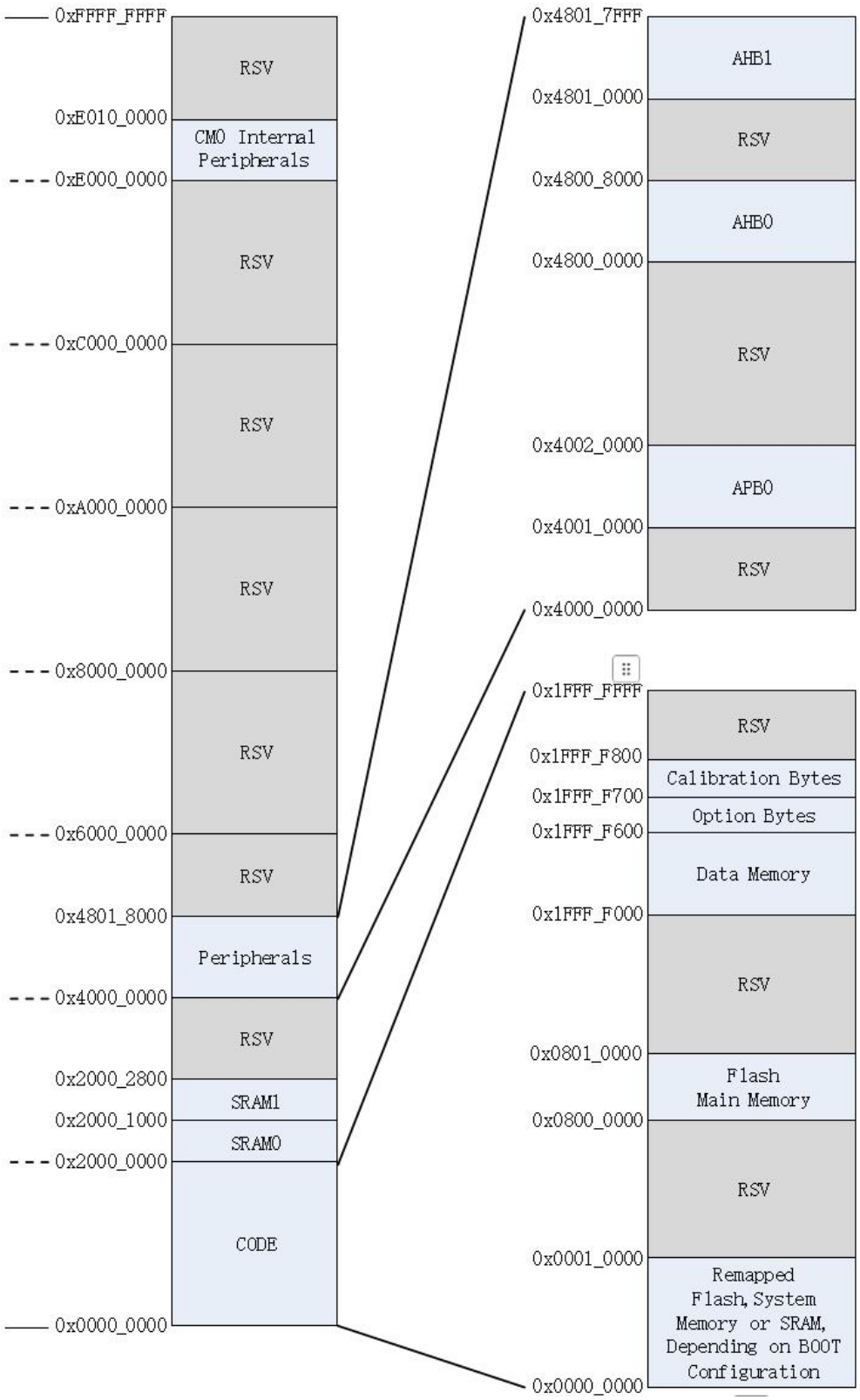


Table 3–1 YTM32M067AS21 Register Boundary Addresses

Bus	Address Area	Size	Peripheral
APB0	0x4001_0000 - 0x4001_0FFF	4KB	TIM1
	0x4001_1000 - 0x4001_1FFF	4KB	EXTI
	0x4001_2000 - 0x4001_2FFF	4KB	Reversed
	0x4001_3000 - 0x4001_3FFF	4KB	I2C0
	0x4001_4000 - 0x4001_4FFF	4KB	USART0
	0x4001_5000 - 0x4001_5FFF	4KB	USART1
	0x4001_6000 - 0x4001_6FFF	4KB	Reversed
	0x4001_7000 - 0x4001_73FF	1KB	CHIPCTRL
	0x4001_7400 - 0x4001_77FF	1KB	IWDG
	0x4001_7800 - 0x4001_7BFF	1KB	WT
	0x4001_7C00 - 0x4001_7FFF	1KB	ANA CTRL
	0x4001_8000 - 0x4001_8FFF	4KB	SPI0
	0x4001_9000 - 0x4001_9FFF	4KB	Reversed
	0x4001_A000 - 0x4001_AFFF	4KB	ADC
	0x4001_B000 - 0x4001_BFFF	4KB	TIM15
	0x4001_C000 - 0x4001_CFFF	4KB	TIM16
	0x4001_D000 - 0x4001_DFFF	4KB	FLASH CTRL
	0x4001_E000 - 0x4001_EFFF	4KB	TIM17
	0x4001_F000 - 0x4001_FFFF	4KB	TIM2
	0x4002_0000 - 0x47FF_FFFF	~128MB	Reversed
AHB0	0x4800_0000 - 0x4800_01FF	512B	GPIOA
	0x4800_0200 - 0x4800_03FF	512B	GPIOB
	0x4800_0400 - 0x4800_05FF	512B	Reversed
	0x4800_0600 - 0x4800_07FF	512B	Reversed
	0x4800_0800 - 0x4800_09FF	512B	Reversed
	0x4800_0A00 - 0x4800_0BFF	512B	Reversed
	0x4800_0C00 - 0x4800_0DFF	512B	Reversed
	0x4800_0E00 - 0x4800_0FFF	512B	Reversed
	0x4800_1000 - 0x4800_1FFF	4KB	Reversed
	0x4800_2000 - 0x4800_2FFF	4KB	Reversed
	0x4800_3000 - 0x4800_3FFF	4KB	Reversed
	0x4800_4000 - 0x4800_4FFF	4KB	DMA
	0x4800_5000 - 0x4800_5FFF	4KB	Reversed
	0x4800_6000 - 0x4800_6FFF	4KB	Reversed
	0x4800_7000 - 0x4800_7FFF	4KB	SYS CTRL
	0x4800_8000 - 0x4800_FFFF	32KB	Reversed
AHB1	0x4801_0000 - 0x4801_0FFF	4KB	CORDIC
	0x4801_1000 - 0x4801_1FFF	4KB	CRC

	0x4801_2000 - 0x4801_2FFF	4KB	Reversed
	0x4801_3000 - 0x4801_3FFF	4KB	Reversed
	0x4801_4000 - 0x4801_4FFF	4KB	Reversed
	0x4801_5000 - 0x4801_5FFF	4KB	DIV
	0x4801_6000 - 0x4801_6FFF	4KB	Reversed
	0x4801_7000 - 0x4801_7FFF	4KB	Reversed

4. Pinouts And Pin Descriptions

SSOP21

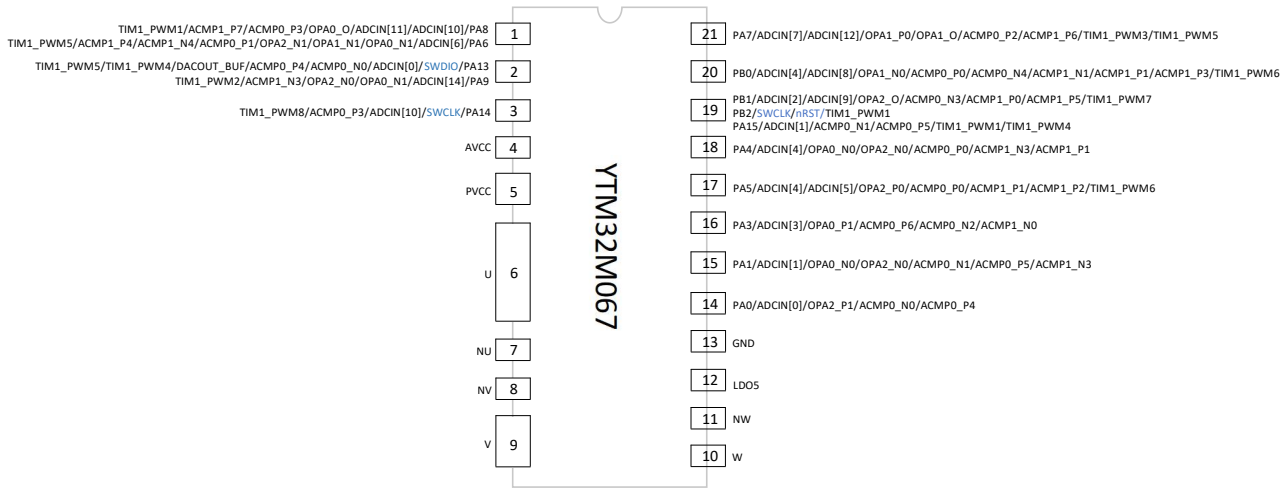


Figure 4-2 Pinout

Table 4-1 Abbreviations Used For Pin Definitions

Name		Abbr.	Description
Pin Name		The pin function and name stay the same during/after reset unless specifically stated in brackets	
Pin Type		P	Power pin
		I	Only input pin
		I/O	Input/output pin
I/O Structure		2ANA	Two analog alternate channels and two normal analog switches (PAD to analog switches with ESD resistance)
		2ANA_OP	Two analog alternate channels, one normal analog switch and one analog switch of low inner resistance
		2OP	Two analog alternate channels and two analog switches of low inner resistance (PAD directly to analog switch for OPA)
Note		All I/Os are floating input during/after reset, unless specified in *Note*	
Pin Function	Optional alternate function	Features configured by GPIOx_AFL/H, GPIOx_MODE registers (digital alternate)	
	External alternate function	Features configured by the SYSCTRL register which has higher priority than optional alternate function (digital alternate)	
	Analog alternate function1	Analog function 1 configured by SYSCTRL or GPIOx_AFL/H, GPIOx_MODE registers	
	Analog alternate function 2	Analog function 2 configured by SYSCTRL or GPIOx_AFL/H, GPIOx_MODE registers	

Table 4-2 YTM32M067AS21 Pin Definitions

Pin Number	Pin Name	Pin Type	I/O Structure	Optional Alternate Function	External Alternate Function	Analog Alternate Function (AN)	
YTM32M067AS21						YA1	YA2
6	U	O		Phase U output, 0V~40V			
	U	O		Phase U output, 0V~40V			
	U	O		Phase U output, 0V~40V			
	U	O		Phase U output, 0V~40V			
5	PVCC	P		Power supply, 6.5V~40V			
	PVCC	P		Power supply, 6.5V~40V			
7	NU	O		Phase U low side S, connecting to ground or shunt resistor, 0V~40V			
9	V	O		Phase V output, 0V~40V			
	V	O		Phase V output, 0V~40V			
	V	O		Phase V output, 0V~40V			
	V	O		Phase V output, 0V~40V			
	V	O		Phase V output, 0V~40V			
	V	O		Phase V output, 0V~40V			
	V	O		Phase V output, 0V~40V			
8	NV	O		Phase V low side S, connecting to ground or shunt resistor, 0V~40V			
10	W	O		Phase W output, 0V~40V			
	W	O		Phase W output, 0V~40V			
	W	O		Phase W output, 0V~40V			
	W	O		Phase W output, 0V~40V			
	W	O		Phase W output, 0V~40V			
11	NW	O		Phase W low side S, connecting to ground or shunt resistor, 0V~40V			
14	PA0	I/O	2ANA_OP	TIM2_CH1 TIM16_CH1 TIM1_ETR TIM15_ETR I2C0_ALERT USART1_RX USART1_CTS ACMP0_out		ADCIN[0] ACMP0_P4 ACMP0_N0 (PA13_YA1)	OPA2_P1

15	PA1	I/O	2ANA_OP	TIM2_CH2 TIM15_CH1N TIM16_CH1N TIM16_CH2 TIM16_ETR I2C0_SDA USART1_RTS USART1_TX		ADCIN[1] ACMP0_P5 ACMP0_N1 OPA1_OX (PA15_YA1)	OPA0_N0 OPA2_N0 ACMP1_N3 (PA4_YA2/ PA9_YA1)
16	PA3	I/O	2ANA_OP	TIM2_CH3 TIM15_CH1 I2C0_SCL USART1_TX USART1_RX SPI0_RXD SPI0_TXD ACMP1_out		ADCIN[3] ACMP0_N2 ACMP0_P6 ACMP1_N0	OPA0_P1
17	PA5	I/O	2ANA_OP	TIM1_PWM6 TIM15_CH1 TIM16_CH2 TIM2_ETR TIM15_ETR I2C0_SCL SPI0_SCK WT_nBuz		ADCIN[4] ACMP0_P0 ACMP1_P1 (PA4_YA1/ PB0_YA1)	ADCIN[5] OPA2_P0 ACMP1_P2
	PVCC	P		Power supply, 6.5V~40V			
13	GND	P		Ground			
18	PA4	I/O	2ANA_OP	TIM15_CH2 TIM17_CH1 USART0_RTS USART1_TX USART1_CK SPI0_FSS ACMP1_out WT_Buz		ADCIN[4] ACMP0_P0 ACMP1_P1 (PA5_YA1/ PB0_YA1)	OPA0_N0 OPA2_N0 ACMP1_N3 (PA1_YA2/ PA9_YA1)
19	PB1	I/O	2ANA_OP	TIM1_PWM7 TIM2_CH4 TIM15_CH1 I2C0_ALERT USART0_RX USART0_TX USART1_RTS		ADCIN[9] ACMP0_N3 ACMP1_P0 OPA2_OX	ADCIN[2] OPA2_O ACMP1_P5 (PA2_YA2)
19	PB2 (nRST)	I/O	2ANA	TIM1_PWM1 TIM2_CH3	SWCLK[2] nRST[3]		

				TIM15_CH2 TIM16_CH1N TIM1/2/15/16/17_GPIO_BKIN USART0_TX USART1_TX			
1	PA6	I/O	2ANA_OP	TIM1_PWM5 TIM2_CH1 TIM16_CH1 TIM1_GPIO_BKIN USART0_CK SPI0_RXD SPI0_TXD ACMP0_out		ADCIN[6] ACMP0_P1 ACMP1_N4	OPA0_N1 OPA1_N1 OPA2_N1 ACMP1_P4 (PA12_YA1)
21	PA7	I/O	2OP	TIM1_PWM3 TIM1_PWM5 TIM2_CH2 TIM17_CH1 USART0_RX SPI0_RXD SPI0_TXD ACMP1_out		ADCIN[7] OPA1_P0 ACMP0_P2	ADCIN[12] OPA1_O ACMP1_P6
	GND	P		Ground			
20	PB0	I/O	2ANA_OP	TIM1_PWM6 TIM2_CH3 USART0_RX USART0_TX EVENTOUT		ADCIN[4] ACMP0_P0 ACMP1_P1 (PA4_YA1/ PA5_YA1)	ADCIN[8] OPA1_N0 ACMP1_P3 ACMP1_N1 ACMP0_N4
1	PA8	I/O	2ANA_OP	TIM1_PWM1 TIM15_CH2 TIM16_GPIO_BKIN TIM17_ETR USART0_TX USART0_CTS ACMP0_out MCO		ADCIN[10] ACMP0_P3 OPA0_OX ELVI[4] (PA14_YA1)	ADCIN[11] OPA0_O ACMP1_P7
2	PA9	I/O	2ANA_OP	TIM1_PWM2 TIM15_CH1 TIM15_CH2N TIM15_GPIO_BKIN		OPA0_N0 OPA2_N0 ACMP1_N3 (PA1_YA2/ PA4_YA2)	ADCIN[14]

				TIM16_GPIO_BKIN I2C0_SCL USART0_RX USART0_TX			
	PA10	I/O	2ANA_OP	TIM1_PWM3 TIM1_PWM8 TIM15_CH2 TIM1_GPIO_BKIN TIM17_GPIO_BKIN I2C0_SDA USART0_RX USART0_TX		ADCIN[15] OPA0_P0	DACOUT_BUF (PA13_YA2)
2	PA13	I/O	2ANA	TIM1_PWM4 TIM1_PWM5 TIM16_CH1 I2C0_SDA USART1_RX ACMP1_out IR_OUT	SWDIO[2]	ADCIN[0] ACMP0_P4 ACMP0_N0 (PA0_YA1)	DACOUT_BUF (PA10_YA2)
3	PA14	I/O	2ANA	TIM1_PWM8 TIM1_CH5 TIM17_CH1 TIM1_GPIO_BKIN I2C0_SCL USART1_RX USART1_TX	SWCLK[2]	ADCIN[10] ACMP0_P3 OPA0_OX ELVI[4] (PA8_YA1)	PMU_AOUT (PA15_YA2)
19	PA15	I/O	2ANA	TIM1_PWM1 TIM1_PWM4 TIM16_CH1N TIM17_CH1 TIM1_GPIO_BKIN TIM15_GPIO_BKIN USART1_RX SPI0_FSS		ADCIN[1] ACMP0_P5 ACMP0_N1 OPA1_OX (PA1_YA1)	PMU_AOUT[6] (PA14_YA2)
	GND	P		Ground			
12	LDO5	O		5V LDO output			
4	AVCC	P		LDO power supply, 6.5V~40V			
	PVCC	P		Power supply, 6.5V~40V			

Note1: *According to the option byte configuration, it can be used as a BOOT0 pin during system reset to select the boot mode, then can be used for normal function.*

Note2: *According to the option byte configuration, one of SWCLK (PB2 or PA14) pins and SWDIO (PA13) can be selected during system reset. After that SWDIO pin is pulled up internally and the SWCLK pin is pulled down internally.*

Note3: *After power-on reset, the PB2 pin is configured as an external reset pin nRST by default. If the option byte is configured as SWCLK, PB2 will be used as SWCLK when the chip starts working, meantime the external reset configuration will be automatically turned off, and then configured by software.*

Note4: *ELVI is an external voltage that can be detected by LVD.*

Note5: *The I/O drive strength 4mA/8mA when powered by 3.3V, and 8mA/16mA when powered by 5V.*

Note6: *PMU_AOUTis the power supply observation output of the chip.*

Table 4-3 GPIOA Optional Alternate Function Mapping

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	TIM15_ETR	USART1_CTS	TIM1_ETR	TIM16_CH1	USART1_RX	TIM2_CH1	ACMP0_out	I2C0_ALERT
PA1	TIM16_ETR	USART1_RTS	TIM16_CH1N	TIM2_CH2	USART1_TX	TIM15_CH1N	TIM16_CH2	I2C0_SDA
PA2	TIM15_CH2	USART1_RX	TIM1_PWM4	USART1_TX	TIM1_PWM5	SPI0_TXD	ACMP0_out	SPI0_RXD
PA3	TIM15_CH1	USART1_TX	SPI0_RXD	TIM2_CH3	SPI0_TXD	I2C0_SCL	ACMP1_out	USART1_RX
PA4	SPI0_FSS	USART0_RTS	TIM15_CH2	TIM17_CH1	USART1_CK	Wt_Buz	ACMP1_out	USART1_TX
PA5	SPI0_SCK	TIM16_CH2	I2C0_SCL	TIM15_CH1	TIM1_PWM6	Wt_nBuz	TIM15_ETR	TIM2_ETR
PA6	SPI0_RXD	TIM2_CH1	TIM1_GPIO_BKIN	ACMP0_out	TIM1_PWM5	TIM16_CH1	USART0_CK	SPI0_TXD
PA7	SPI0_TXD	TIM2_CH2	TIM1_PWM5	ACMP1_out	USART0_RX	TIM17_CH1	TIM1_PWM3	SPI0_RXD
PA8	MCO	USART0_CTS	TIM1_PWM1	TIM15_CH2	USART0_TX	TIM16_GPIO_BKIN	ACMP0_out	TIM17_ETR
PA9	TIM15_CH2N	TIM15_GPIO_BKIN	USART0_TX	TIM1_PWM2	I2C0_SCL	TIM16_GPIO_BKIN	TIM15_CH1	USART0_RX
PA10	TIM15_CH2	TIM17_GPIO_BKIN	USART0_RX	TIM1_PWM3	I2C0_SDA	USART0_TX	TIM1_PWM8	TIM1_GPIO_BKIN
PA11	-	I2C0_SDA	TIM1_PWM3	TIM15_CH1	USART0_TX	Wt_Buz	USART0_CTS	-
PA12	-	I2C0_SCL	TIM1_PWM2	TIM15_CH1N	USART0_RX	Wt_nBuz	USART0_RTS	-
PA13	SWDIO	IR_OUT	TIM1_PWM5	TIM1_PWM4	USART1_RX	TIM16_CH1	ACMP1_out	I2C0_SDA
PA14	SWCLK	USART1_TX	TIM1_CH5	TIM1_GPIO_BKIN	TIM17_CH1	TIM1_PWM8	I2C0_SCL	USART1_RX
PA15	SPI0_FSS	USART1_RX	TIM17_CH1	TIM15_GPIO_BKIN	TIM1_PWM1	TIM16_CH1N	TIM1_GPIO_BKIN	TIM1_PWM4

Table 4-4 GPIOB Optional Alternate Function Mapping

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	EVENTOUT	TIM2_CH3	TIM1_PWM6	-	USART0_TX	-	USART0_RX	-
PB1	TIM15_CH1	TIM2_CH4	TIM1_PWM7	-	USART1_RTS	USART0_RX	I2C0_ALERT	USART0_TX
PB2	SWCLK	TIM1/2/15/ 16/17_GPIO_ BKIN	TIM1_PWM1	TIM2_CH3	TIM15_CH2	TIM16_CH1N	USART1_TX	USART0_TX
PB3	SPI0_SCK	TIM1_PWM5	TIM1_PWM7	TIM16_CH1	TIM16_ETR1	TIM1_PWM8	TIM1_PWM1	USART1_TX
PB4	SPI0_RXD	TIM2_CH1	TIM1_PWM6	USART0_RX	TIM1_PWM7	TIM17_GPIO _BKIN	TIM16_CH2	SPI0_TXD
PB5	SPI0_TXD	TIM2_CH2	TIM1_PWM8	TIM1_PWM3	USART0_TX	TIM1_PWM4	TIM1_PWM6	SPI0_RXD
PB6	USART0_TX	I2C0_SCL	TIM16_CH1N	TIM15_CH2	TIM1_PWM5	TIM1_PWM1	TIM2_CH3	USART0_RX
PB7	USART0_RX	I2C0_SDA	TIM17_CH1N	TIM1_PWM6	USART0_TX	TIM1_PWM3	TIM17_CH1	TIM1_PWM2
PB8	TIM17_ETR	TIM1_PWM5	TIM1_PWM2	TIM1_PWM3	TIM15_CH2	TIM16_CH1	TIM17_CH1N	I2C0_ALERT

Table 4–5 YTM32M067AS21 Internal Pin Connection

Internal Connection	Pin Description	Example of corresponding TIM1 PWM functions	
PB3	The logic input control signal is active at high, and control Phase U MOS high–side: "0" is to turn off the power MOS, "1" is to turn on the power MOS.	AF5	TIM1_PWM8
PB7	The logic input control signal is active at high, and control Phase V MOS high–side: "0" is to turn off the power MOS, "1" is to turn on the power MOS.	AF5	TIM1_PWM3
PB8	The logic input control signal is active at high, and control Phase W MOS high–side: "0" is to turn off the power MOS, "1" is to turn on the power MOS.	AF2	TIM1_PWM2
PB6	The logic input control signal is active at high, and control Phase U MOS low–side: "0" is to turn off the power MOS, "1" is to turn on the power MOS.	AF4	TIM1_PWM5
PB5	The logic input control signal is active at high, and control Phase V MOS low–side: "0" is to turn off the power MOS, "1" is to turn on the power MOS.	AF6	TIM1_PWM6
PB4	The logic input control signal is active at high, and control Phase W MOS low–side: "0" is to turn off the power MOS, "1" is to turn on the power MOS.	AF4	TIM1_PWM7

4. Recommended Application Circuit

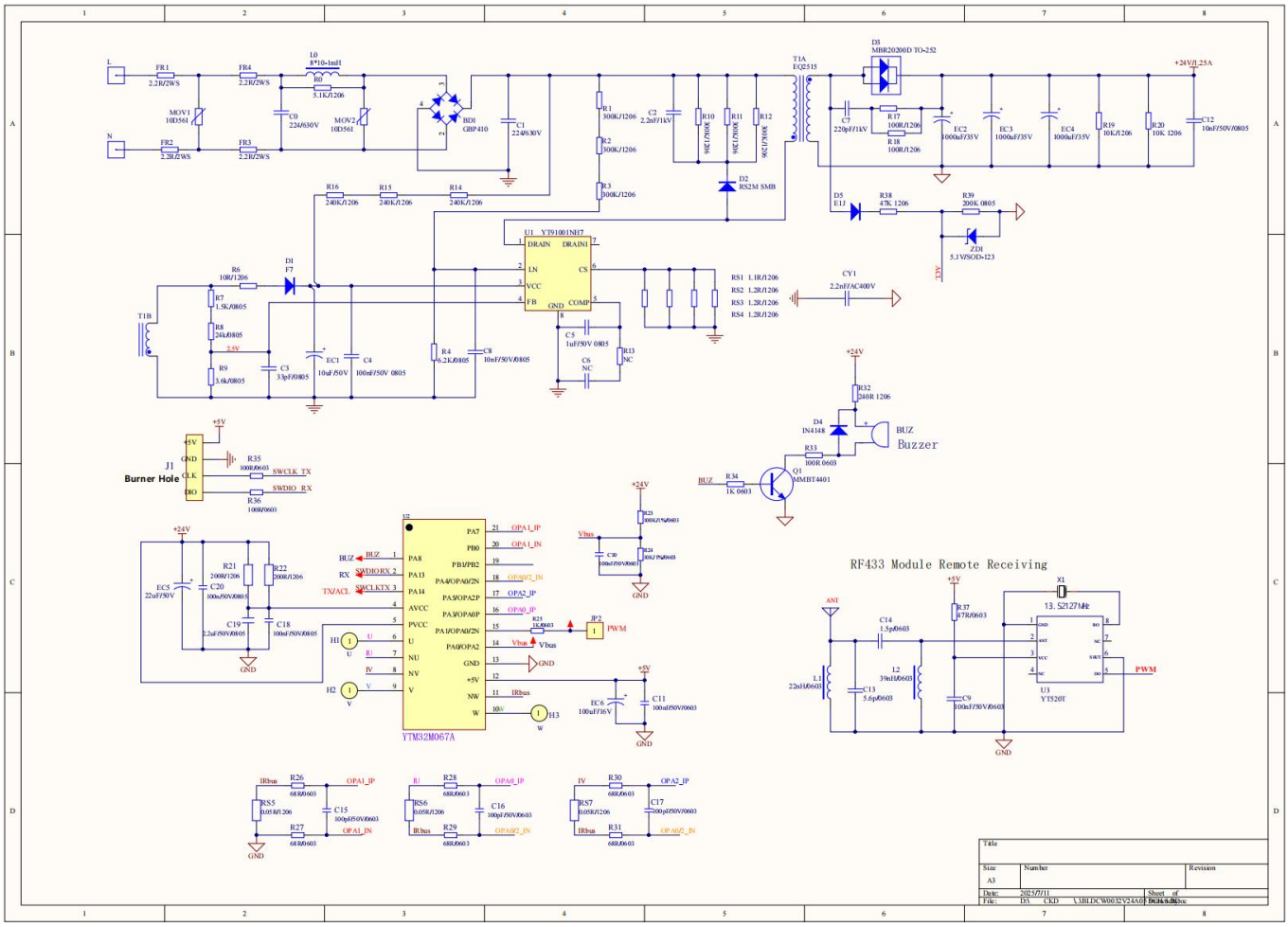


Figure 5–1 YTM32M067AS21 Application Connection Diagram

6. Electrical Characteristics

6.1 Absolute Characteristics

Table 6–1 YTM32M067AS21 Absolute Characteristics

Parameter	Symbol	Min.	Max.	Unit
AVCC/PVCC supply voltage	VCC	–0.3	40	V
LDO output voltage	V_{LDO}	–0.3	6	V
LDO output current	I_{LDO}	0	50	mA
Junction temperature	T_J	–40	150	°C
Storage temperature	T_{STG}	–40	150	°C

Note: *Stresses above the absolute maximum values may cause permanent damage to the device. Exposure to maximum value conditions for extended periods may affect device reliability.*

6.2 Typical Characteristics

Unless otherwise specified, T_A=25°C, VCC=30V, load capacitance C_L=1nF.

Table 6–2 YTM32M067AS21 Typical Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	VCC	_	5.0	-	28	V
VCC turn–on voltage	VCC_{on}	_	3.8	4.5	5	V
VCC under–voltage protection threshold	VCC_{UVLO}	_	3.6	4.3	4.8	V
VCC quiescent current	I_{VCC_S}	HIN and LIN floating	-	500	-	uA
LDO output voltage	V_{LDO}	_	4.85	5	5.15	V
LDO output current	I_{LDO_LMT}	_	-	40	50	mA
input signal frequency	f_{IN}		0	-	50	kHz
Over–temperature protection threshold	T_{OTP}	_	_	150	_	℃
Resetting over–temperature protection	T_{OTP_R}	_	_	135	_	℃

6.3 Electrical Characteristics of the Controller

6.3.1 Absolute Maximum Ratings

Permanent damage to the device may occur if operated beyond the "absolute maximum values." These values are only extreme operating conditions; operation outside this range is not recommended. Long-term operation at maximum values will affect reliability.

Table 6–3 Voltage Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power Supply Voltage	VDDH/VDDA	-0.3	3.3/5	6.5	V
I/O InputVoltage	VIN	-0.3	3.3/5	5.8	V

Note: All voltages are referenced to VSS.

Table 6-4 Current Characteristics

Parameter	Symbol	Test Condition	Minimum Value	Typical Value	Maximum Value	Unit
Total current flowing into VDDH/VDDA	$\sum I_{VDD}$	-	-	-	120	mA
Total current flowing out of VSS/VSSA	$\sum I_{VSS}$	-	-	-	-120	
Maximum current of each VDDH/VDDA pin	I_{VDD} (pin)	-	-	-	100	
Maximum current of each VSS/VSSA pin	I_{VSS} (pin)	-	-	-	-100	
Pin injection current	I_{INJ}	$V_{IN}>V_{DD}$或$V_{IN}<V_{SS}$	-10	10	20	
Total injection current	ΣI_{INJ}	-	-50	-	50	

Table 6-5 Thermal Characteristics

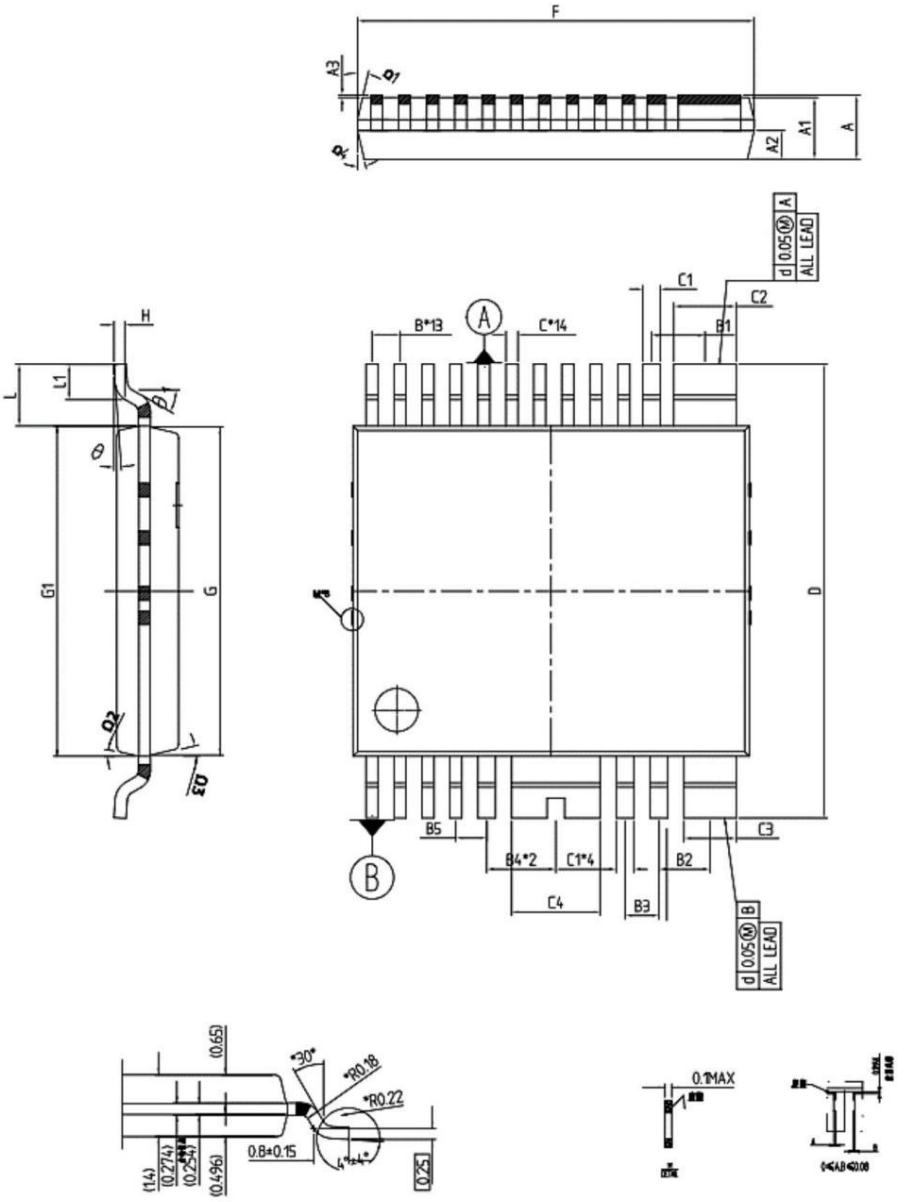
Parameter	Symbol	Minimum Value	Typical Value	Maximum Value	Unit
Storage temperature range	T_{STG}	-40	25	150	℃
Maximum junction temperature	T_J	-40	25	150	

6.3.2 Recommended Operating Conditions

Table 6-6 Operating Conditions

Parameter	Symbol	Test Condition	Minimum Value	Typical Value	Maximum Value	Unit
Operating voltage	VDDH	-	2.0	3.3/5	5.5	V
Analog operating voltage	VDDA	>= VDDH	2.0	3.3/5	5.5	V
I/O input voltage	V_{IN}	-	-0.3	-	5.5	V
CPU frequency	f_{CPU}	VDDH＞2.0V	-	-	108	MHz
AHB clock frequency	f_{AHB}	-	-	-	108	MHz
APB clock frequency	f_{APB}	-	-	-	48	MHz
VDDH/VDDA rise rate	t_{VRISE}	-	0	-	∞	us/V
VDDH/VDDA fall rate	t_{VFALL}	-	20	-	∞	us/V
Power dissipation	P_D	T_A = 25℃	-	500	-	mW
Ambient temperature	T_A	-	-40	-	125	℃

7. Packaging

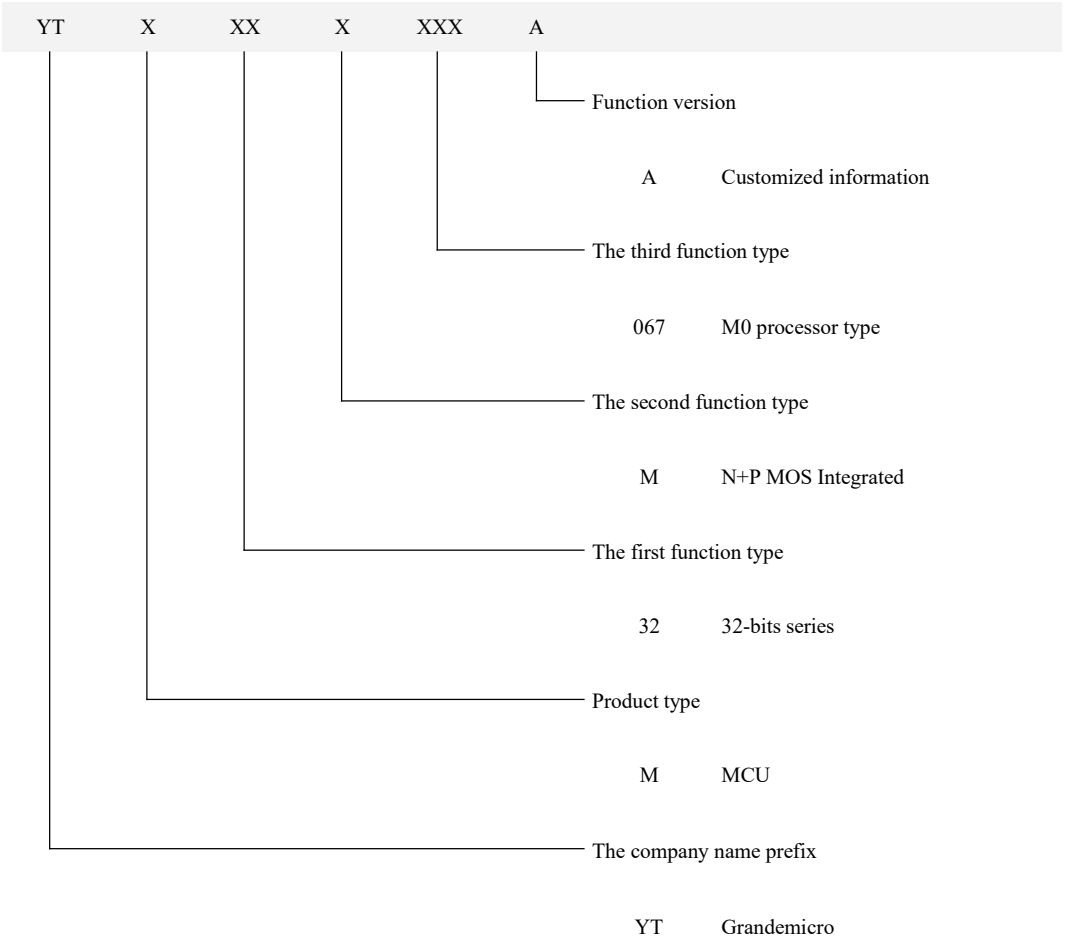


SYMBOL	MILLIETER(mm)		
	MIN	NOM	MAX
A	1.4200	1.4600	1.5200
A1	1.3500	1.4000	1.4500
A2	0.6000	0.6500	0.7000
A3	0.0200	0.0700	0.1200
B	–	0.6350	–
B1	–	1.2075	–
B2	–	1.1575	–
B3	–	0.7700	–
B4	–	1.5700	–
B5	–	0.7000	–
C	–	0.2700	–
C1	–	0.4000	–
C2	–	1.4150	–
C3	–	1.1850	–
C4	–	2.0100	–
D	–	10.3000	–

F	8.9500	9.0000	9.0500
G	7.4000	7.4500	7.5000
G1	7.4500	7.5000	7.5500
L	–	1.4000	–
L1	0.6500	0.8000	0.9500
H	–	0.2500	–
Ω1	–	13°	–
Ω2	–	13°	–
Ω3	–	13°	–
Ω4	–	13°	–
θ	0°	4°	8°
θ_1	–	30°	–

Figure 7–1 Package information

8. Ordering Information



9. Revision History

Table 9–1 Revision History

Date	Rev.	Description
2025.07.30	A0	First released
2026.01.16	A1	Have corrected the errors in individual units in the table, and adjusted the parameters related to some temperature ranges